DESIGN AND FABRICATION OF FREE-STANDING STRUCTURES AS OFF-CHIP INTERCONNECTS FOR MICROSYSTEMS PACKAGING

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DESIGN AND FABRICATION OF FREE-STANDING STRUCTURES AS OFF-CHIP INTERCONNECTS FOR MICROSYSTEMS PACKAGING

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SUMMARY

It is projected by the Semiconductor Industry Association in their International Technology Roadmap for Semiconductors (ITRS) that by the year 2019, with the IC feature size shrinking to about 10 nm, off-chip interconnects in an area array format will require a pitch of 95 μm. Also, as the industry transitions to porous low-K dielectric materials/Cu interconnects, it is important to ensure that the stresses induced by the off-chip interconnects and the package configuration do not crack or delaminate the low-K dielectric material. Compliant free-standing structures used as off-chip interconnects are a potential solution. However, there are several design, fabrication, assembly and integration research challenges and gaps with the existing suite of compliant interconnects. Accordingly, as part of this research an innovative multiple electrical path approach to compliant interconnects was developed. Such an approach is shown to enhance the mechanical compliance of the interconnects without compromising the electrical parasitics. It also provides for redundancy and thus result in increased reliability of interconnects. Also, as part of this research, a variable compliance approach is developed so that the interconnects near the center of the die have lower electrical parasitics while the interconnects near the edge/corner of the die have higher mechanical compliance. Such an integrated approach is shown to be capable of improving electrical performance without compromising on mechanical performance. Furthermore, in this work a fabrication process is developed which facilitates cost-effective, high-yield, and uniform fabrication of free-standing compliant interconnects and critical factors which impact assembly yield of free-standing compliant interconnects are investigated. The experimental reliability of free-standing compliant interconnects are also investigated as part of this research. Ultimately the proposed approaches are demonstrated by developing

an innovative compliant interconnect called FlexConnects. Hence, the compliant interconnects developed through this research are expected to address the needs of first level interconnects over the next decade. This would eliminate a bottleneck that threatens to impede the exponential growth in microprocessor performance. Also, the concepts developed are generic in nature and can be extended to other aspects of electronic packaging for improved electrical performance and/or mechanical reliability.

CHAPTER 1
INTRODUCTION

Gordon Moore of Intel observed that historically chip functionality (number of bits/transistors) doubles every 1.5 to 2 years. This observation is popularly known as Moore's law (Figure 1.1) and has continued to drive the semiconductor industry over the past decades. Moore's law has been primarily sustained by consistently reducing transistor size and cost per transistor, consequently increasing the number of transistors on a chip. An increase in the number of transistors drives an increase in the number of off-chip interconnects needed to connect a chip to other components of an electronic system (Off-chip interconnects refer to interconnects between the chip and the substrate). Furthermore, reducing the transistor size increases transistor density. This results in more transistors per chip for the same chip size. Thus the increased number of off-chip interconnects must be accommodated in the same area i.e. off-chip interconnect density must also increase. Hence, it is projected by the Semiconductor Industry Association in their International Technology Roadmap for Semiconductors (ITRS) that by the year 2019, with the IC feature size shrinking to about 10 nm, off-chip interconnects in an area array format will require a pitch of 95 μm [ITRS 2007].

Off-chip interconnects must also be compatible with other advances being made by the semiconductor industry. High performance microprocessors and computers are increasingly being limited by power and latency. Power refers to both supplying the power and dissipating it. Global interconnects on the IC (integrated circuit) span at least half a chip edge. Latency is caused by the consequent RC (Resistance-Capacitance) and transmission line delay [Ho et al. 2001]. Limits on chip power dissipation, power density and hyper-pipelining in microprocessors threaten to impede the exponential growth in microprocessor performance. Multi-core processors represent a viable solution that can continue to provide a historical performance growth. To sustain the dramatic performance

growth, a rapid increase in the number of cores per die and a corresponding growth in off-chip bandwidth are required [Hofstee 2004]. In other words, adoption of an I/O centric multi-core architecture demands an increase in the number of off-chip interconnects at increasingly finer pitches. Furthermore, to reduce the RC and transmission line delay, low-K dielectric/Cu and ultra-low-K dielectric/Cu interconnects on silicon will become increasingly common. In such IC's, the thermo-mechanical stresses induced by the off-chip interconnects could crack or delaminate the dielectric material causing reliability problems. Hence, it is desirable that off-chip interconnects reduce the stresses introduced in the die.

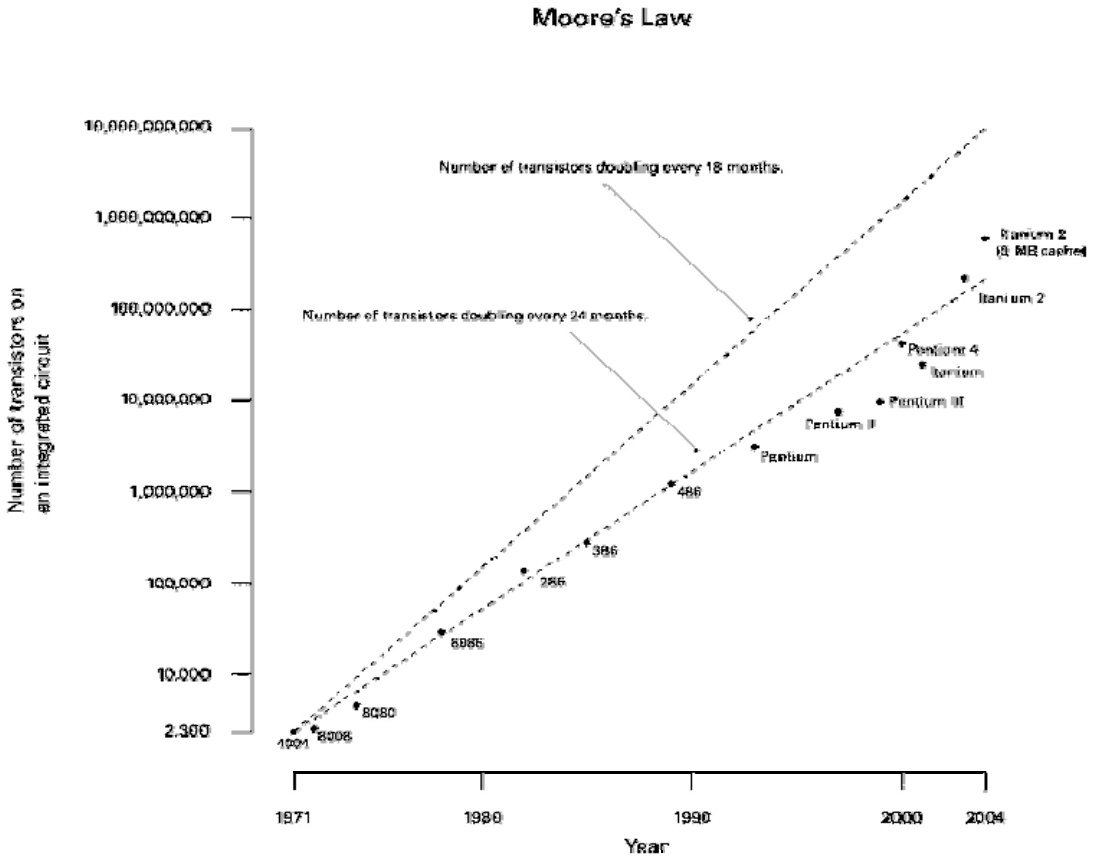


Figure 1.1: Moore's Law [Wikimedia 2004]

Table 1.1: International Technology Roadmap for Semiconductors (ITRS) [ITRS 2007]

Year of Production	*2009*	*2011*	*2013*	*2016*	*2019*	*2022*
DRAM ½ Pitch (nm) (contacted)	*50*	*40*	*32*	*23*	*16*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*52*	*40*	*32*	*23*	*16*	*11*
MPU Physical Gate Length (nm)	*20*	*16*	*13*	*9*	*6.3*	*4.5*
Flip Chip Area Array Pitch (μm)	130	120	110	110	95	90

Conventional off-chip interconnects include wire bonding, Tape Automated Bonding (TAB), and C4 bumps. Wire bonding is widely used but is inherently incapable of addressing the high I/O count, fine-pitch off-chip interconnect requirements because they are not area array. TAB is an improvement over wire-bonding in the sense that it supports gang bonding. However it is more costly and suffers from the same drawbacks as wire bonding in its inability to support an area-array of interconnects. Flip chips with solder bumps are being increasingly used today due to their several advantages: higher I/O density, shorter leads, lower inductance, higher frequency, better noise control, smaller device footprint, and lower profile [Lau 1996]. Epoxy-based underfills are often used in such flip chip assemblies to accommodate the coefficient of thermal expansion (CTE) mismatch among different materials (e.g. silicon IC on an organic substrate) and to enhance the solder joint reliability against thermo-mechanical fatigue failure [Viswanadham and Singh 1998; Tummala 2001]. However, additional underfill process steps, material and processing costs, reworkability, delamination, and cracking are some of the concerns with the use of underfills. Also, as the pitch size decreases, the cost and the difficulties associated with underfill dispensing will increase dramatically [Chi Shih et al. 1998; Ghaffarian 1998].

Furthermore, when low-K dielectric (ultra low-K dielectric in the future) is used in the silicon IC and when such ICs are assembled on organic substrates, the chip-to-substrate interconnects are subjected to extensive differential displacement due to the CTE mismatch between the die and the substrate under thermal excursions. The interconnects, especially stiff solder bumps, could crack or delaminate the low-K dielectric material in the die. In addition, if the solder bumps are not underfilled, they will fatigue crack and fail prematurely.

Alternatively, a compliant interconnect structure can be utilized to accommodate the CTE mismatch between the silicon die and the organic substrate. Such an approach decouples the die from the substrate and eliminates the need for an underfill material. This is in contrast to the solder bump approach which utilizes an underfill material to couple the die to the substrate to ensure interconnect reliability. Elimination of the underfill material makes compliant interconnect amenable to fine pitch assemblies and allows for reworkable interconnects. Also, compliant interconnects exert minimal force on the die pads, and therefore, will not crack or delaminate the low-K dielectric material on the die. However, compliant interconnects suffer from certain drawbacks and are yet to be implemented commercially. Primary concerns with compliant interconnects are their relatively high cost of fabrication and their high electrical parasitics, especially inductance. In addition, there is limited information regarding the assembly processes that would need to be utilized for such interconnects and the reliability of packages assembled with such interconnects. Therefore, it is necessary to explore alternate interconnects that are compliant so that it will not crack or delaminate the low-K dielectric, that it will not fatigue fail prematurely without an underfill, that it is easy to fabricate and assemble using existing infrastructure, that it is scalable, that is wafer-level, and that it will meet the electrical and mechanical requirements for next-generation microsystems.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

An electronic system is made up of both active and passive devices. Interconnects connect these active and passive devices to realize a functional electronic system. Interconnects in an electronic system have two primary functions: signal distribution and power distribution. To fulfill these functions, interconnects are present at various levels of an electronic system and can be categorized into the hierarchy shown in Table 2.1.

Table 2.1: Hierarchy of Interconnects

Level 0	Interconnects within a single chip to connect devices within the chip. Referred to as on-chip interconnects.
Level 1	Interconnections between an individual chip and the first level of packaging. This could be the package substrate or in some cases could be directly to a printed wiring board. Referred to as off-chip interconnects / chip-to-substrate interconnects / chip-to-next-level interconnects / chip level interconnects.
Level 2	Interconnections between an individual package and the printed wiring board.
Level 3	Interconnections between individual printed wiring boards.
Level 4	Interconnections between sub-assemblies.
Level 5	Interconnections between two physically distinct systems.

The focus of this research is on Level 1 interconnects. Section 2.2 provides a description of the requirements of first level interconnects. Section 2.3 describes conventional first level interconnects. Section 2.4 describes different compliant interconnect technologies.

2.2 First Level Interconnect Requirements

A viable first level interconnect technology should address the following challenges

a. Mechanical reliability: The interconnect must have sufficient compliance to not delaminate or crack low-K dielectric. It must also have sufficient thermo-mechanical reliability to pass standard qualification tests without the use of an underfill material.

b. Low electrical parasitics: Interconnects should meet the high digital speed (~20 GHz) and high data rate (4-10 Gbs/channel) requirements for future ICs. Inductance in the neighborhood of 0.06 nH and resistance in the neighborhood of 30mΩ are desirable for power-ground interconnects at the operating frequencies. For signal interconnects, in addition to the resistance and inductance requirements, the parasitic capacitance should be less than 0.1 pF at 4Gbps [Kim et al. 2003].

c. Cost effective fabrication process: To be cost effective, it is preferable that the proposed interconnects be batch fabricated at the wafer-level (large-area fabrication), not at the IC-level. The fabrication and assembly of interconnects should be easily integrated into existing infrastructure, and the processes should be repeatable with a good yield. Also, the interconnects should be reworkable, and therefore, it is preferable not to use underfill. If a solder is to be used for interconnect attachment, it should be environmentally-friendly lead-free solder.

d. Fine pitch and scalable with IC feature size: As IC feature size scales from 20nm in 2009 to 7nm in 2019 [ITRS 2007], the first level interconnect pitch goes down from 130μm in 2007 to 95μm in 2019 (area-array configuration) [ITRS 2007]. Hence a compliant interconnect which addresses today's needs must be scalable to address future pitch requirements.

2.3 Conventional First Level Interconnects

There are three principal first level interconnect technologies currently in use

a. Wirebonding

b. Tape automated bonding (TAB)

c. Flip chip / C4

Wirebonding is the oldest of these three technologies and currently the most widely used. A typical wirebond is shown in Figure 2.1. Wirebonding involves sequentially connecting the die pad on the chip to a corresponding pad on a metal frame / substrate using a thin wire. This thin wire, referred to as the wirebond, is attached at either end by thermosonic and/or ultrasonic welding methods. Prior to the wirebond being formed, the backside of the chip is attached to the metal frame or substrate using a suitable die attach material. Wirebonding has numerous advantages. The foremost is that it is a mature technology with the necessary infrastructure in place. Consequently, wirebonding is a robust and reliable technology. Also, it is a flexible process as the same wirebonding equipment can be reused for a variety of products through a simple reprogramming operation. However, wirebonds can only be formed along the chip edge and hence, they cannot support a full area array of interconnects. This factor along with the serial fabrication procedure means that they cannot support a high I/O count. Also, the wirebond loops have high electrical parasitics and a large package footprint.

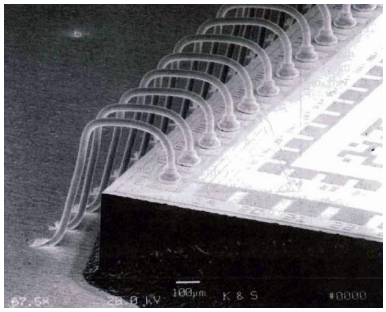


Figure 2.1: Wire Bonds (Courtesy K&S)

Tape automated bonding (TAB) was developed in the 1960's to address the problems with wirebonds. In the 1960's wirebonding was still a nascent technology with poor reliability which was unable to cost effectively realize a large number of I/O's. TAB uses metal coated polymer beams fabricated on a polymer tape. A three layer tape is shown in Figure 2.2. The chips are bumped with a suitable metallurgy to which the metallized polymer beams are attached. This is followed by testing, encapsulation, singulation and burn-in. The chip with the tape leads is then attached to the next level of the package. TAB, unlike wirebonding, allows simultaneous formation of the interconnects and improves electrical performance of the interconnects as the wire bond loops are eliminated. However, TAB is relatively expensive and cannot support current and future high density I/O requirements as it is not area array. Electrical parasitics, though lower than wire bonds, are still unacceptably high due to long parallel interconnects. Also, the package footprint is large.

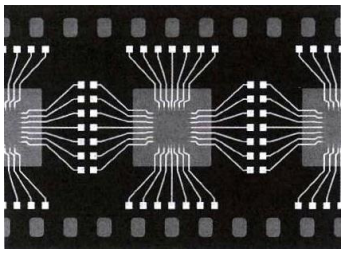


Figure 2.2: 28 Lead Three-layer Tape for TAB (Courtesy of Shindo Densi Ltd.)

The flip chip process was developed by IBM in the 1960's to overcome the poor reliability and expense associated with wirebonding. The flip chip process in the 1970's evolved into the C4 (Controlled Collapse Chip Contact) technology. In the flip chip process, unlike wirebonding and TAB, the active circuitry of the chip faces down. A low temperature melting material, typically some type of solder is deposited on the die pads of the chip with suitable interface metallurgies. Dies bumped with solder are shown in Figure 2.3. The chip with the solder material is then assembled onto a substrate by reflowing the solder material. Flip-chips are gaining increased acceptance both for cost-

performance as well as high-performance applications. Flip chip has a number of advantages: higher I/O density, shorter leads, lower inductance, higher frequency, better noise control, smaller device footprint, and lower profile [Lau 1996]. However, to ensure the reliability of the solder joint an epoxy based underfill material must be used. The underfill material is dispensed between the chip and the substrate and then cured. However, additional underfill process steps, material and processing costs, reworkability, delamination, and cracking are some of the concerns with the use of underfills. Also, as the pitch size decreases, the cost and the difficulties associated with underfill dispensing will increase dramatically [Chi Shih et al. 1998; Ghaffarian 1998]. First level interconnects are subjected to extensive differential displacement due to the CTE mismatch between the die and the substrate under thermal excursions. When low-K dielectric (ultra low-K dielectric in the future) is used in the die the interconnects, especially stiff solder bumps, could crack or delaminate the low-K dielectric material. Furthermore, if the solder bumps are not underfilled, they will fatigue crack and fail prematurely.

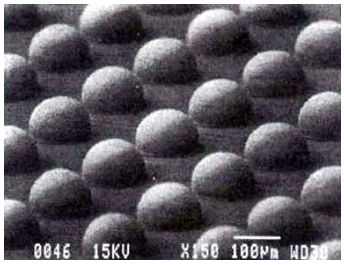


Figure 2.3: Electroplated Solder Bumps for Flip-Chip [Magill et al. 1996]

An approach similar to the flip chip process based on copper bumps is also being pursued. Such an approach has been adopted by Intel [DeBonis 2007] along with other companies. An example is shown in Figure 2.4. Essentially this is the same as the flip chip process, except that copper is used as the bump material instead of solder. Assembly is performed using a solder material and an underfill is dispensed between the chip and the substrate. One of the advantages of this approach over conventional flip chip

is the improved electromigration resistance of the interconnect as the current is more uniformly distributed. The other advantage is that it is a completely lead-free technology. As it is similar to solder based flip chip, the other advantages and disadvantages are similar.

Conductive adhesives are an alternative given the move of industry to lead-free solders, but processing difficulties restrict them to low I/O density applications. Commercial use of conductive adhesives is typically restricted to LCD devices.

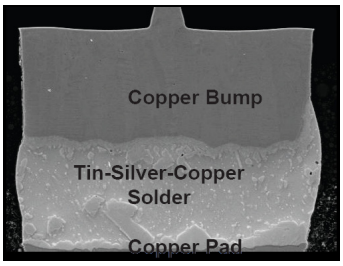


Figure 2.4: Intel's Copper Bump Technology [DeBonis 2007]

2.4 Compliant First Level Interconnects

2.4.1 FormFactor's MOST™

FormFactor had developed a compliant interconnect element called MicroSpring™ based on wirebonding. MicroSpring™ was first used in probe card applications. A typical MicroSpring™ interconnect for probe card applications is shown in Figure 2.5. FormFactor extended this technology to realize a WLP (Wafer Level Package) which utilized the MicroSpring™ interconnect as a first level interconnect. This application of the MicroSpring™ interconnect was called MOST™ (MicroSpring contact On Silicon Technology) [Novitsky and Pedersen 1999]. MOST utilizes a modified wirebonder to realize free standing compliant interconnects on a silicon wafer. Once formed, the wirebond is plated with suitable metals. The interconnect shape is determined by controlling the motion of the wirebonder. The interconnects are assembled either by socketing or soldering. Though a successful technology for probe card applications

MOST has had limited success as a first level interconnect. This can be attributed to the MOST fabrication process. The serial nature of the fabrication process is not viable for large I/O counts. Also, such a fabrication process is unable to achieve fine I/O pitches.

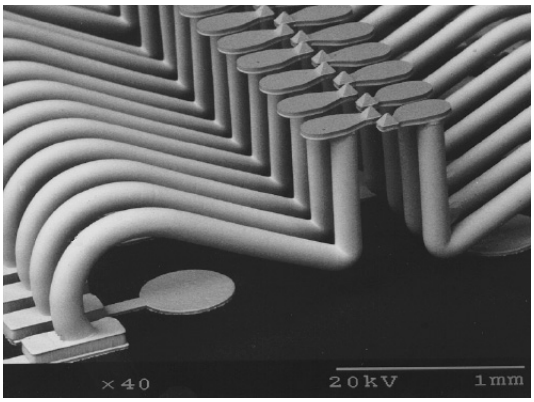


Figure 2.5: FormFactor's MicroSpringTM Technology [Novitsky and Pedersen 1999]

2.4.2 Tessera's µBGA® and WAVE

Tessera's µBGA® [DiStefano and Fjelstad 1996] is a compliant Chip Scale Package (CSP) based on flexible circuit technology. The µBGA® package uses a patterned polyimide flexible circuit with metal leads. The flexible circuit is attached to the die using an elastomer which is a few mils thick. Leads attached along the edge of the flexible circuit, are then thermosonically bonded, in a sequential manner, to the die pads present along the periphery of the chip. The polyimide flexible circuit has traces that fan-in from the metal leads to pads on the flexible circuit layer. The package can then be bumped at the pads and assembled using standard SMT (Surface Mount Technology) techniques. Compliance between the chip and the substrate is provided by the metal leads and the low modulus elastomer. The leads and the elastomer combine to take up the CTE mismatch between the die and the substrate. Hence, no underfill is required for the solder bumps. Two drawbacks of the µBGA® package are the low compliance of the leads and the use of a sequential bonding process.

Tesseara's introduced its second generation of compliant packages called Wide Area Vertical Expansion (WAVE) [Fjelstad 1998; Young-Gon et al. 2001] to overcome some of the limitations of the µBGA® package. A cross-section of a WAVE package is shown in Figure 2.6. The WAVE package utilizes leads with greater compliance than those used in the µBGA® package. This enables greater reliability and an ability to address larger die sizes as compared to a µBGA® package. Also, the WAVE package allows for gang bonding of the leads to the die, enabling a larger number of I/O's and more flexibility in die pad location. The WAVE package is again based on polyimide flexible circuits but utilizes a different fabrication process compared to the µBGA® package. A two layer polyimide flexible circuit is used with leads fabricated on it. Special attention is paid to the lead design to increase lead slack and hence improve reliability. The leads on the flexible circuit have a suitable bonding material deposited at their end. First, leads are attached to die pads on the silicon and hence partially released from the surface of flexible circuit. An elastomeric material is then injected between the flexible circuit and the die, vertically raising the leads attached between the flexible circuit and the die. The compliant leads along with the elastomeric material provide the necessary compliance to decouple the die from the substrate. Similar to the µBGA® package, the flexible circuit can now be bumped and then assembled using standard SMT processes. WAVE represents an improvement over µBGA® by batch processing interconnects that have a higher compliance. However, the compliance is still limited due to the use of an encapsulating elastomer.

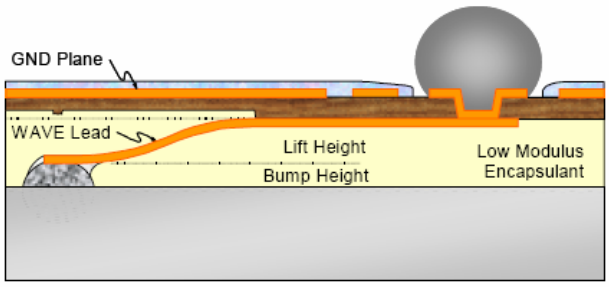


Figure 2.6: WAVE Package Cross-Section [Young-Gon et al. 2001]

2.4.3 Floating Pad Technology (FPT)

Floating pad technology (FPT) enables pads on a device to move freely in all three direction (*x, y,* and *z*) [Fillion et al. 2001] and hence be compliant. This is achieved by fabricating pads on a "micro-pocket". A schematic representation of FPT is shown in Figure 2.7. To realize the "micro-pocket", a photodefinable compliant layer is spun on the wafer / chip carrier. Openings are defined at locations where the micro-pockets are desired. A polymer film is then attached, covering the micro-pocket. Pads, along with suitable routing, are defined on the polymer film, on top of the micro-pocket. The pads also include an annular ring which sits on the compliant polymer film, outside of the micro-pocket area. The pads connect to the annular ring through thin metal lines, which allow the pad to remain compliant. The pads are bumped and the solder bumps now sit on a compliant micro pocket which improves their reliability. Limitations of this technology include an inability to realize fine-pitch interconnect due to the fabrication process utilized. Also, the interconnects would not have a high compliance.

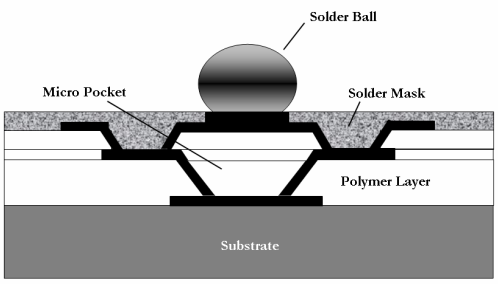


Figure 2.7: FPT Cross-Section [Fillion et al. 2001]

2.4.4 Sea of Leads (SoL)

Sea of Leads compliant interconnects evolved from the Compliant Wafer Level Package (CWLP) developed at Georgia Tech [Patel et al. 2000]. CWLP was based on batch-fabrication of interconnects at the wafer level. Such an approach allowed for a potentially low-cost interconnect solution which could support a high interconnect density. However, the CWLP interconnects were fabricated on a polymer layer which

reduced the compliance of the interconnects. Sea of Leads were developed to address some of the limitations of CWLP. In one implementation of SoL, (Figure 2.8) leads were fabricated with embedded air gaps to increase their compliance [Reed et al. 2001]. The air gap was realized by defining a sacrificial material in the regions where an air gap was desired. An overcoat polymer material was spun on top of the sacrificial material and then the sacrificial material was thermally decomposed, realizing the air gap. The interconnects were then fabricated on top of the air gap. In another implementation of SoL interconnects (Figure 2.9), interconnects were realized with a partial length of the interconnect having reduced adhesion to the underlying polymer layer [Bakir et al. 2003]. This improved the compliance of the interconnects and hence these interconnects were called "slippery" SoL. A third implementation of SoL (Figure 2.10) utilizes a sacrificial layer to realize interconnects which are free standing and hence, have higher compliance [Dang et al. 2006]. Even though SoL continually improved its compliance through innovations in fabrication, it was limited by its design which impaired the realization of an interconnect with sufficient compliance.

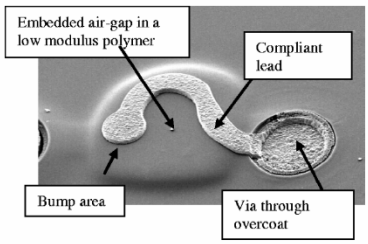


Figure 2.8: Sea of Leads with Embedded Air Gap [Bakir et al. 2003]

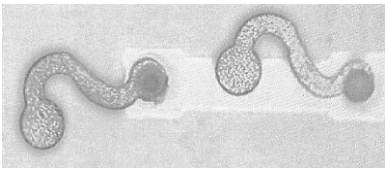


Figure 2.9: Slippery Sea of Leads, Interconnect on the Left is Displaced by the Application of a Lateral Force [Bakir et al. 2003]

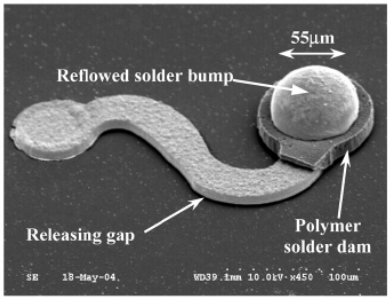


Figure 2.10: Sea of Leads with Releasing Gap for Free-Standing Interconnects [Dang et al. 2006]

2.4.5 Helix Interconnects

Helix interconnects are a lithography-based electroplated compliant interconnect that can be fabricated at the wafer level and were developed at Georgia Tech. Helix interconnects were the first compliant interconnects that were free-standing, which enabled them to have a high compliance. A Design of Experiments (DOE) approach followed by an optimization process was utilized to develop the Helix interconnect design. This allowed Helix interconnects to have excellent mechanical performance without compromising on their electrical characteristics. An implementation of Helix interconnects called "G-Helix" interconnects is shown in Figure 2.11 [Zhu et al. 2004]. As seen, the G-Helix interconnect consists of an arcuate beam and two end posts. The arcuate beam is incorporated into the design to accommodate the differential displacement in the planar directions (x and z). The two vertically-off-aligned end posts connect the arcuate beam to the die and to the substrate and provide compliance in the three orthogonal directions. The fabrication of G-Helix interconnects is based on the lithography, electroplating and molding (LIGA-like) technologies, and can be integrated into wafer-level fine-pitch batch processing. Another implementation of Helix interconnects called β-Helix is shown in Figure 2.12 [Zhu et al. 2003]. Compared to the G-Helix interconnects, β-Helix has improved mechanical performance but at the price of reduced electrical performance and an increase in the number of fabrication steps. G-

Helix interconnects would be more suitable for consumer products characterized by a relatively benign field-use conditions. β-Helix interconnects would be more suitable in harsh-environment applications. Drawbacks associated with Helix interconnects include the somewhat involved fabrication process and the use of a long RIE etch for photoresist removal as part of the fabrication procedure.

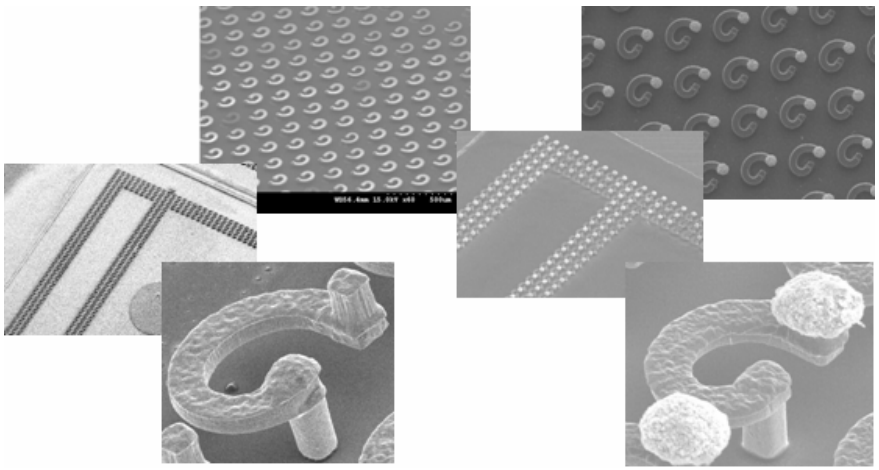


Figure 2.11: 100-µm and 200-µm Pitch G-Helix Interconnects Fabricated on a Silicon Wafer

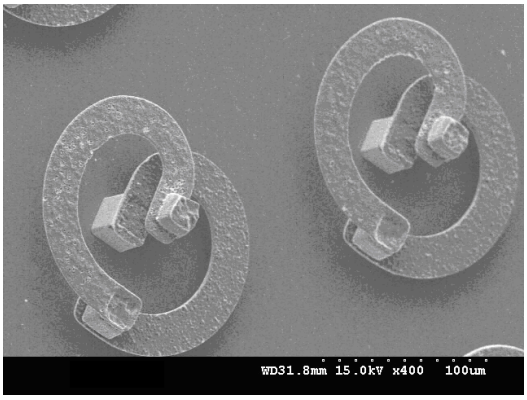


Figure 2.12: β-Helix Interconnects Fabricated on a Silicon Wafer

2.4.6 Stress-Engineered Interconnects

A consortium comprising PARC, Georgia Tech, and NanoNexus had developed linear and J-like stress-engineered compliant interconnects. These interconnects are

fabricated using DC sputtering to realize intrinsically stressed structures which curl off the surface of the wafer and are shown in Figure 2.13 [Smith and Alimonda 1996; Smith et al. 1998; Ma et al. 2002]. To fabricate them, the interconnect metal is sputter deposited at a low Argon pressure on a patterned sacrificial layer. By changing the Argon pressure, a stress gradient can be introduced into the metal. Once the sacrificial layer supporting the metal is removed, the intrinsic stress causes the metal to curl up in the regions where the sacrificial layer was present. The interconnects are anchored to the die at locations where the sacrificial layer was not present. Such an approach allows for batch fabrication of the interconnects. Assembly of the interconnect is only through contact and does not require solder. The interconnect is sufficiently compliant to not require an underfill and can support very fine pitch interconnects (up to 6μm). However, the use of a non-standard sputtering fabrication process is a drawback and also results in interconnects which are not uniform across the wafer. To address this, replacing the sputtering process by an electroplating process has been explored [Chow et al. 2005].

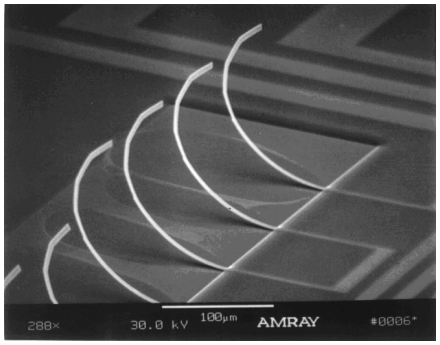


Figure 2.13: J-Spring Stress-Engineered Interconnects Fabricated on a Silicon Wafer

2.4.7 Nano-Structured Copper Columns

A nano-structured copper column approach attempts to utilize the advantages of a copper column and overcome the low compliance of the copper column by utilizing nano-grained copper. The advantages of using a copper column as a first-level

interconnect are many [Tummala et al. 2006]. Primary among these advantages is improved electrical performance due to the use of copper and a short electrical connection. Also, such an approach is easily integrated with back-end processing. Copper columns also have improved resistance to electromigration due to lower joule heating, ability to support higher current densities and more uniform current distribution. These advantage have led to the adoption of copper column interconnects. For example, Intel utilizes such an approach in their products. However, to guarantee interconnect reliability an underfill material is utilized, with its associated disadvantages. To eliminate the use of the underfill, nano-structured copper columns have been advocated [Tummala et al. 2006]. Nano-structured copper is deposited using an electrochemical process. The morphology or grain refinement of the plated copper can be controlled by adding suitable additives to the aqueous copper sulfate based plating solution. Nano-structure copper has been shown to have superior fatigue resistance compared to coarse grained copper. This allows nano-structured copper columns to take up the CTE mismatch between the substrate and the die without the use of an underfill material. The primary concern with such an approach is the method by which the interconnects are attached. If low temperature solder is utilized then the stiff nano-structured copper columns transfer the strains to the solder, causing it to fail prematurely. In other words, though the interconnect is protected due to the use of nano-structured copper, a new failure mode is introduced defeating the advantages of using nano-structured copper. Solid state copper to copper bonding could be utilized. However, this has its own disadvantages like higher processing temperature and need for high substrate planarity.

2.4.8 Sea of Polymer Pillars (SoPP)

Sea of Polymer Pillars (SoPP) utilizes mechanically compliant high aspect ratio polymer pins as electrical and optical interconnects [Bakir et al. 2007]. These are shown in Figure 2.14. The use of the polymer material allows the interconnects to have high

compliance. The polymer material allows for transmission of optical signals, unlike any of the other compliant interconnects described. Also the polymer pins improve optical efficiency over free-space optical interconnects as optical transmission through air is avoided. For the purpose of conducting electrical signals a thin layer of metal is coated on the polymer pins. Metal coated polymer pins are shown in Figure 2.15. In this manner, the same interconnect can transmit both optical and electrical signals. However, metal coated polymer pillars have a high optical loss. These interconnects are fabricated using wafer level batch processes. Extending SoPP to a 'trimodal' wafer level package is also being explored [Bakir et al. 2007]. In this configuration the polymer pins perform a third function as fluidic I/O's. To achieve this hollow I/O's are fabricated which transport a cooling fluid to support on-chip cooling. These are shown in Figure 2.16. The ability of these interconnects to perform three functions simultaneously makes them a promising interconnect technology. A concern with SoPP is if the metal coated polymer pins would have sufficient compliance to be reliable.

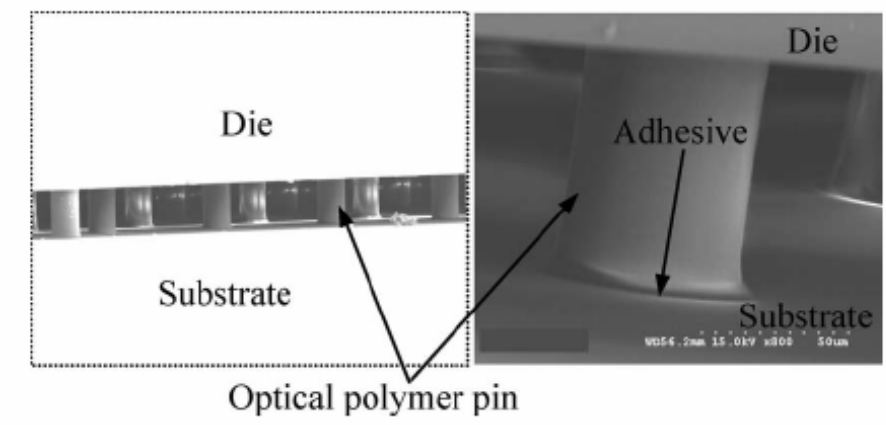


Figure 2.14: Assembled Optical Polymer Pins [Bakir et al. 2007]

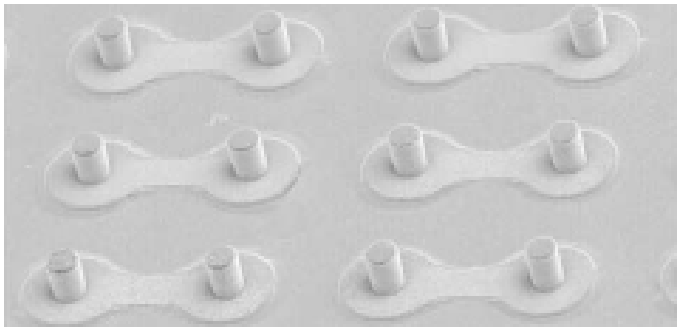


Figure 2.15: Polymer Pins with a 3µm Gold Coating [Bakir et al. 2007]

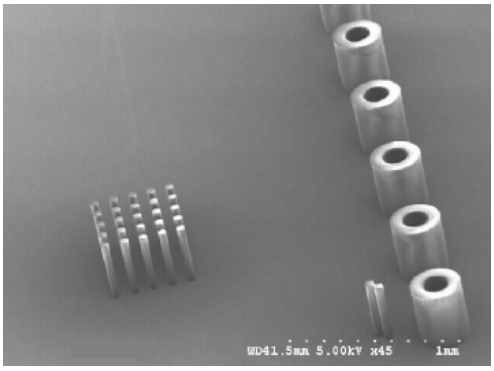


Figure 2.16: Optical I/O's Fabricated Adjacent to Fluidic I/O's [Bakir et al. 2007]

2.4.9 Elastic-bump on Silicon Technology (ELASTec®)

Elastic-bump on Silicon Technology (ELASTec®) is based on a resilient polymer bump with a metal lead plated on it [Dudek et al. 2006]. The polymer bump provides the compliance and the metal lead provides the electrical connection. An ELASTec bump with spiral metal lead is shown in Figure 2.17. A wafer level packaging approach is adopted. The polymer (silicone) is printed on the wafer and the metal leads are defined through lithography. The metal leads are soldered onto the printed circuit board(PCB). No underfill material is utilized. ELASTec has been demonstrated to pass a number of standard reliability tests [Dudek et al. 2005]. However, ELASTec was developed as a second-level interconnect for memory applications which are characterized by a low I/O count. It would appear that this technology would be unable to satisfy fine pitch requirements due to limitations of the fabrication process adopted. Also the interconnect

would not be able to achieve sufficient compliance at a fine pitch for a reliable connection.

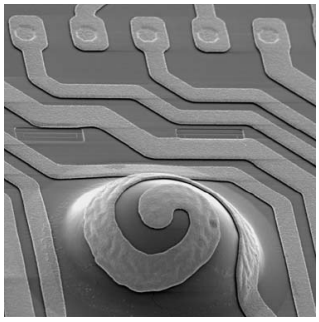


Figure 2.17: ELASTec® Bump with Spiral Metal Lead [Dudek et al. 2005]

CHAPTER 3
OBJECTIVES AND SCOPE OF RESEARCH

3.1 Gaps in Existing Research

Based on the literature review conducted, it is seen that the following research gaps exist with utilizing compliant structures as off-chip interconnects:

a. Mechanical Compliance: The recommended target for mechanical compliance is 7 mm/N in the three orthogonal directions [Intel-Corporation 2001]. Such a compliance will ensure that the interconnect will not crack or delaminate the low-K dielectric material in current and future dies and will easily accommodate high CTE organic substrates. It would also aid in wafer probing. Compliant interconnects such as SoL, WAVE, ELASTec do not meet this target in the planar or out-of-plane direction. Interconnects based on nano-crystalline material are clearly very stiff and cannot meet the compliance targets.

b. Electrical Parasitics: All of the proposed compliant interconnects have high electrical parasitics compared to solder bumps. The existing body of literature does not adequately address how to overcome this without compromising the mechanical compliance of the interconnect. Compliant interconnects such as MicroSpring™, SoL, G-Helix have inductance values which are significantly higher than comparable solder bumps. Other approaches like SoPP, stress-engineered springs have high electrical resistance.

c. Assembly: Several of the proposed compliant interconnects cannot be easily assembled. For example, stress-engineered springs cannot be assembled without the solder wetting the entire structure. Sea of Leads have been assembled but at a relatively coarse pitch of 300μm pitch and only after the introduction of additional processing steps to prevent wetting of the entire interconnect. The assembly of G-Helix interconnects is yet to be

demonstrated. It is important to determine the appropriate load, flux, solder volume, and reflow profile to be able to successfully assemble compliant interconnects at a fine pitch (100μm).

d. Cost-effective and High-Yield Fabrication: Although compliant interconnects offer several advantages over conventional solder bumps, unless they can be fabricated cost effectively and with high yield, their implementation will be limited. Stress-engineered springs do not have high yield and cannot be fabricated uniformly across the wafer. Stress-engineered spring also call for a non-standard fabrication process. Sea of Leads when implemented with an air gap calls for an unconventional fabrication process. With interconnects based on nano-crystalline materials it is difficult to get a stable grain size which remains nanoscale. G-Helix has a high fabrication cost due to the three-mask process.

3.2 Objectives, Approaches, and Scope of Work

3.2.1 Objective

Clearly, there are several design, fabrication, assembly, and integration research challenges and gaps with the existing suite of compliant interconnects. The objective of this research is to address these limitations of the current suite of compliant interconnect by developing mutually compatible concepts pertaining to the design, fabrication, and assembly of compliant interconnects. This would enable compliant interconnects to address the needs of off-chip interconnects over the coming decade (discussed in Section 2.2) and hence be a viable alternative. The concepts developed, will be integrated to realize a compliant interconnect technology called FlexConnects. With respect to the design of the interconnects, concepts will be developed both at the level of the individual interconnect as well as at the system level which allow for improved electrical performance without compromising on mechanical performance. With respect to the

fabrication of the interconnects, a MEMS based approach will be utilized to develop an innovative fabrication process which utilizes a minimum number of fabrication steps and is compatible with existing infrastructure of the semiconductor industry.

3.2.2 Approaches

To achieve the objectives stated above, this dissertation aims to:

1. develop an innovative parallel-path/multiple-path approach to compliant interconnects. Such an approach will enhance the mechanical compliance of the interconnects without compromising the electrical parasitics. Also, such an approach will provide for redundancy and thus will result in more reliable interconnects.
2. develop a variable compliance approach so that the interconnects near the center of the die have lower electrical parasitics while the interconnects near the edge/corner of the die have higher mechanical compliance. Such an integrated approach will be able to meet both electrical and mechanical performance requirements.
3. investigate critical factors which impact assembly yield of free-standing compliant interconnects and utilize this information to develop an assembly process recipe for free-standing compliant interconnects.
4. develop a fabrication process which will facilitate cost-effective, high-yield, and uniform fabrication of free-standing compliant interconnects
5. demonstrate the proposed approaches by developing an innovative compliant interconnect called FlexConnects

3.2.3 Scope of Work

Although the concepts developed in this dissertation will be utilized to develop a compliant interconnect called FlexConnects, these concepts are generic in nature and can

be extended with relative ease to other compliant interconnect technologies. In particular, the concepts developed regarding the design of compliant interconnects have implications to other scenarios where a displacement controlled load exists. For example, a number of structures utilized in electronic packaging experience a displacement controlled load and the concepts developed in this dissertation can be applied to them.

CHAPTER 4
DESIGN OF COMPLIANT INTERCONNECTS

4.1 Introduction

A first-level interconnect is a physical structure which conducts electricity from the chip to the substrate. The ability of an interconnect to fulfill this function is determined by its electrical and mechanical performance characteristics which in turn are determined by the interconnect design. This dissertation proposes to utilize, a "compliant interconnect" between the chip and the substrate. A significant limitation of such an interconnect is its inferior electrical performance characteristics when compared to a solder bump. Though the dimensions of a compliant interconnect can be modified to improve its electric performance, this would be at the expense of the mechanical performance, and hence, may not always be a viable alternative. Therefore, a design concept which allows an improvement in the electrical performance without compromising the mechanical performance would be desirable. Using such a concept a new compliant interconnect design can be developed which would be expected to have improved performance characteristics, making compliant interconnects a more viable alternative to conventional off-chip interconnects.

This chapter describes the development of such a design concept which involves the utilization of multiple electrical paths as part of the compliant interconnect design. First, the design constraints imposed on compliant interconnects are described (Section 4.2). Subsequently, the new design concept is introduced and its benefits are described through an analytical model (Section 4.3). Next, the applicability of this new design concept to column interconnects is discussed (Section 4.4). Then, a description of a new compliant interconnect design called single-path FlexConnect is provided (Section 4.5) and its performance is characterized through numerical models (Section 4.6). The new design concept is then applied to the single-path FlexConnect design to realize the parallel-path FlexConnect and through numerical models the improved performance of

the parallel-path FlexConnect is highlighted (Section 4.7). In developing the design of the parallel-path / single-path FlexConnect, care is taken to ensure that it is compatible with the fabrication process developed in Chapter 5. To demonstrate the generic nature of the design concept, it is implemented on a previously developed compliant interconnect technology called Sea of Leads (Section 4.8). Finally, a more detailed modeling of the electrical performance of parallel-path FlexConnects is performed (Section 4.9).

4.2 Design Criteria for Compliant Interconnects

As described in Section 2.2, there are four primary requirements for compliant interconnects – mechanical performance, electrical performance, fine pitch and cost effective fabrication. The fabrication process imposes an overall constraint on realizable compliant interconnect designs. A second constraint imposed on the interconnect design is that of the pitch required. This limits the size of the interconnect. The pitch required also determines if the fabrication process can be utilized as certain fabrication techniques are not amenable for interconnects at a fine pitch. As this dissertation aims to address the needs of interconnects at a fine pitch (100μm), photolithography enabled fabrication processes will be utilized. Photolithography enables the cost-effective batch fabrication of fine features. As photolithography is utilized, it restricts the interconnect to planar structures but enables a wide variety of 2D geometries and also allows for scalability with interconnect pitch. A detailed description of the fabrication process is provided in Chapter 5. The remaining two constraints, electrical performance and mechanical performance, represent the fundamental functions of a compliant interconnect – a compliant mechanical structure which conducts electrical signals while accommodating the CTE mismatch between the substrate and the die. These are discussed in greater detail in the following two sub-sections.

4.2.1 Mechanical Design of Compliant Interconnects

The mechanical function of a compliant interconnect has two interrelated components – sufficient compliance and mechanical reliability. Compliance measures the amount a structure deforms per unit of the applied force. If one were to assume the interconnect to be fixed at one end, the directional compliance can be obtained by applying forces in the orthogonal *x*, *y* and *z* directions at the other end. From the resulting displacements u_x, u_y, and u_z, the directional compliance C_x $(= u_x / F_x)$, C_y $(= u_y / F_y)$, and C_z $(= u_z / F_z)$ can be obtained. A free standing first level interconnect deforms due to the CTE mismatch between the silicon die and the organic substrate. For such a displacement controlled load, compliance determines the force applied by the interconnect. The higher the compliance, the lower is the force applied by the interconnect and the lower is the stress in die. This decreases the probability that the interconnect will crack or delaminate the low-K dielectric used in the die. It is hence desirable to have a higher compliance. Based on reliability concerns (low-K dielectric cracking) the compliant interconnect should have an in-plane compliance of around 7 mm/N [Intel-Corporation 2001]. This is greater than two orders of magnitude when compared to conventional solder bumps. Such a high compliance is required as the interconnects must accommodate the CTE mismatch between the die and the substrate without the use of an underfill material.

However, when the reliability of the interconnect is considered, the compliance of the interconnect by itself is not a sufficient metric. For the displacement controlled load experienced by a free-standing interconnect, the amount of energy stored in the interconnect as it deforms is a function of the compliance. The higher the compliance, the lower is the amount of energy stored in the interconnect which increases interconnect reliability. However, the distribution of energy within the interconnect is also important. If more energy is concentrated in particular regions of the interconnect, those regions will

fail first. Hence, the geometry of the interconnect is important as it determines the manner in which energy is distributed within it. Therefore, a design which results in an interconnect having a high compliance is a necessary though not a sufficient condition. The design must also realize an interconnect that has sufficient reliability.

Another key characteristic of compliant interconnects is that they are typically not rotationally symmetric like solder joints. Consequently the in-plane compliance of the interconnects differs depending upon the direction in which the displacement is applied. Ideally we would like the interconnects to experience a displacement in a direction in which their compliance is greatest. For a die assembled on a substrate the center of the die represents the neutral point i.e. the point at which the die does not move relative to the substrate when a thermal load is applied. A line drawn from the center of the die to the compliant interconnect is the direction in which the compliant interconnect deforms. It is hence desirable to orient the interconnect in such a manner that this line is in the direction in which the interconnect compliance is the greatest. Such an approach allows maximal use of the interconnect compliance and should be taken into consideration while designing the package. This concept is utilized when designing the test vehicle as described in Chapter 5 of this dissertation.

4.2.2 Electrical Design of Compliant Interconnects

An electronic package serves two key electrical functions – signal distribution and power supply / grounding. The electrical characteristics of the first level interconnect influence these functions by affecting the signal distortion, signal speed and degradation of the power supply.

Three key parameters of a compliant first-level interconnect which influence its electrical function are its resistance, inductance and capacitance. The first parameter, the resistance of the interconnect causes it to dissipate electrical power as heat resulting in localized joule heating. In addition, a higher value of resistance increases the probability

of electromigration. Localized joule heating further exacerbates the phenomenon of electromigration. Electromigration is not desirable as it negatively impacts interconnect reliability. Finally, the resistance of the interconnect also has an impact on RC delay, a lower resistance, resulting in a smaller RC delay. Hence, it is desirable to minimize the resistance of the interconnect. The second parameter, inductance is possibly the most significant parasitic of a compliant interconnect. Compliant interconnects in general have a relatively high inductance. This is a direct consequence of their compliant design which typically results in structures with long metal lines and consequently a high inductance. Parasitic inductances along with parasitics capacitance can result in cross-talk i.e. signals appearing in parts of the circuit where they should not exist. More importantly, parasitic inductances cause the degradation of power supply. When circuits transition, these parasitic inductances result in the supply voltage oscillating about the DC voltage. They hence contribute to simultaneous switching noise, resulting in a fluctuation of the supply voltage on the power supply rails. Such voltage fluctuation can result in false switching of circuits. In the future, the tolerable inductance of an interconnect will decrease for the following reason. As the rates at which circuits switch increase, for the same inductance, the voltage fluctuation increases. At the same time voltage and signal levels are decreasing with a consequent decrease in power supply budget. Hence, a combination of these factors requires a reduction in the inductance of an off-chip interconnect. It would be desirable to bring the inductance of a compliant off-chip interconnect as close as possible to that of an equivalent solder joint. For interconnects at a 100μm pitch, solder bumps have an inductance of around 20-25 pH [Kim et al. 2003]. The third parameter, the capacitance of a compliant interconnects arises in part from the metal conductors of the interconnect and the ground circuitry. Stray capacitances are also introduced by the physical proximity of other interconnects [Swaminathan et al. 2001]. Capacitance contributes to the RC delay which can be a limiting factor on the speed of the system. Mutual capacitance also contributes to cross-talk. It would hence be desirable to reduce

the capacitance. Regarding capacitance, at 4 Gbs a target value of 0.1pF or below is desirable [Kim et al. 2003]. However, the capacitance of compliant interconnects is not a significant cause for concern because its value is expected to be low. One reason for the low value is that for a free-standing compliant interconnect, the surrounding medium, air, has a low dielectric constant resulting in a lower value for capacitance. Additionally, due to the micron scale dimensions of these interconnects, the surface area of the compliant interconnect parallel to other conductors is small and hence results in a smaller value for its capacitance. Hence the capacitance of the interconnect is expected to be small compared to that of other parts of the interconnection between the driving and receiving circuits.

In general, it is desirable to reduce the electrical parasitics of compliant interconnects. However, in [Braunisch et al. 2004], it is shown that the inductance associated with compliant interconnects is beneficial to a certain extent when they are used as high-speed signal interconnects. This is because they provide some benefit in the context of compensating for the pad capacitance. Pad capacitance refers to the capacitance of the electrostatic discharge (ESD) protection diodes, on-die routing, bumps/leads attached to pads and the driving and receiving circuits. These add up to a total shunt capacitance for the die-package interface between the on-die drivers and receivers. However, the electrical parasitics of the compliant interconnect needed to enable this compensation of the pad capacitance is dependent on the signal frequency and would involve optimizing the parasitics based on the frequency. It is not clear if this is a feasible approach. Hence, the design of compliant interconnects is approached with the intention of minimizing the electrical parasitics but with an understanding that the electrical parasitics of the interconnect are not always harmful.

4.2.3 Trade-off between Mechanical and Electrical Performance

It is desirable to reduce the electrical parasitics of compliant interconnects and increase their mechanical compliance and reliability. However, in general it is seen that when a change is made to the geometry of the compliant interconnect to improve the electrical performance it is at the expense of the mechanical performance of the compliant interconnect and vice-versa. Such results have been shown for the Helix interconnects in [Zhu et al. 2003; Zhu et al. 2004]. Hence, any performance gain from a mechanical perspective is offset by the decrease in performance from an electrical perspective and vice-versa. A design concept which allows an improvement in mechanical performance without detrimentally impacting electrical performance would be useful and would increase the range of applications for which compliant interconnects can be utilized. Such a concept is described in the following section and the advantages of such an approach are illustrated utilizing an analytical model.

4.3 Compliant Interconnects with Multiple Electrical Paths

Almost all compliant interconnect technologies developed previously employ a single electrical path [DiStefano and Fjelstad 1996; Fjelstad 1998; Smith et al. 1998; Novitsky and Pedersen 1999; Patel et al. 2000; Ma et al. 2002; Bakir et al. 2003; Zhu et al. 2003; Zhu et al. 2004; Dang et al. 2006; Dudek et al. 2006; Bakir et al. 2007]. However, by utilizing multiple electrical paths as part of the interconnect design it is possible to enhance the mechanical performance without detrimentally impacting the electrical performance. To illustrate this, as an example, consider a semi-circular beam, which similar to a compliant interconnect, has both an electrical and a mechanical function. The beam (Figure 4.1a) experiences a mechanical load due to a force F and also conducts a current i from one end of the beam to the other. The beam has a square cross-section with its height and its width equal to a. Using Euler-Bernoulli beam theory and

assuming small deflections, it can be shown that for a cantilevered beam with a point load applied at its end

$$\delta = K' \frac{FL^3}{I} \qquad \textbf{(4.1)}$$ [Gere and Timoshenko 1997]

where δ is the displacement at the end of the beam, L is the length of the beam, I is the moment of inertia of the beam cross-section, and K is a constant of propotionality. The compliance C of the beam is then

$$C = \frac{\delta}{F} = K' \frac{L^3}{I} \qquad \textbf{(4.2)}$$

For the beam described in Figure 4.1, the moment of inertia is given by

$$I = \frac{a^4}{12}$$
$$\Rightarrow C = 12K' \frac{L^3}{a^4} \qquad \textbf{(4.3)}$$

The electrical resistance R of the structure is inversely proportional to its cross-section area A and is given by

$$R = K'' \frac{1}{A} = K'' \frac{1}{a^2} \qquad \textbf{(4.4)}$$

Now, the beam is cut through the middle along its length (Figure 4.1b), creating two electrical paths. The second path is mirrored, creating a circular geometry. The moment of inertia I of each individual beam is now

$$I = \frac{\left(\frac{a}{2}\right)^3 \times a}{12} = \frac{a^4}{96} \qquad \textbf{(4.5)}$$

And the compliance for the both beams together is

$$C' = \frac{1}{\frac{a^4}{96K'L^3} + \frac{a^4}{96K'L^3}} = 48K' \frac{L^3}{a^4} \qquad \textbf{(4.6)}$$

The resistance of both beams together is now

$$R' = K'' \left(\frac{1}{a \times \frac{a}{2}} + \frac{1}{a \times \frac{a}{2}} \right) = K'' \frac{1}{a^2} \qquad \textbf{(4.7)}$$

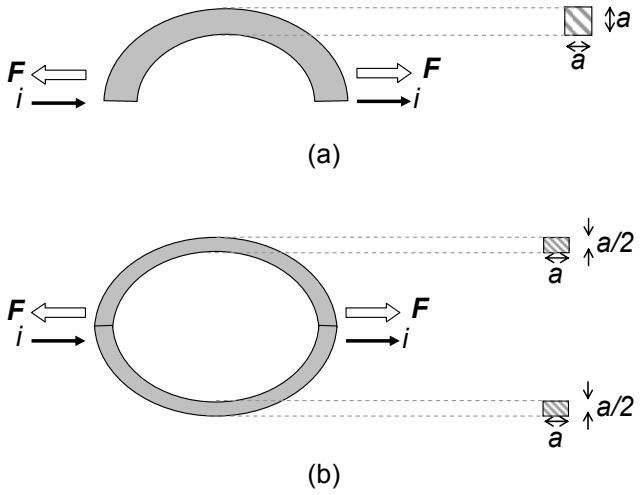


Figure 4.1: Beam Structure Dimensions

Hence

$$\frac{C'}{C} = 4$$
$$\frac{R'}{R} = 1 \qquad \textbf{(4.8)}$$

This means that the electrical resistance remains the same, whereas the compliance is four times its previous value. Hence by using two electrical paths, an opportunity exists to achieve the same electrical performance as the single-path interconnect while obtaining an improved mechanical compliance. Stated differently, using parallel-path (i. e. two-path) compliant interconnects, if one were to keep the mechanical compliance the same as single-path interconnect, the electrical performance of the parallel-path interconnect will be superior compared to the single-path interconnect. Another advantage of utilizing more than one electrical path is that it provides for a redundant design. One of the electrical paths can fail, but the interconnect can continue functioning albeit at the expense of reduced electrical performance.

Extending the concept of using two electrical paths, three or more electrical paths can also be utilized. The number of electrical paths is limited by the ability to fabricate the structure. Using this concept a new compliant interconnect design can be developed

and is described in Section 4.7. Also, this concept is generic in nature and can be applied to most other compliant interconnect technologies as demonstrated in Section 4.8.

4.4 Multiple Columns

Before utilizing the multiple-path concept to develop a new compliant interconnect design, the case of a simple column used as a compliant interconnect is considered. One of the simplest realizations of the multiple electrical path concept is to utilize a multitude of columns to replace a single columnar interconnect. Based on the concept described in Section 4.3 we would expect to achieve a high compliance value utilizing such an approach. This concept is illustrated in Figure 4.2. Figure 4.2a illustrates a single column interconnect between the chip and the substrate. Figure 4.2b illustrates multiple column interconnects between the chip and the substrate. However, as shown in the following paragraphs, for fine pitch interconnects, multiple columns are not necessarily advantageous.

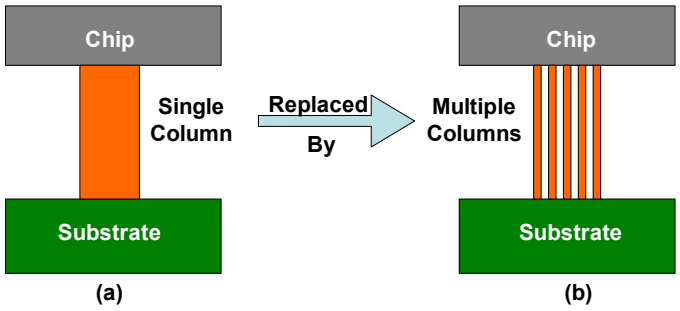


Figure 4.2: Multiple Copper Columns as an Interconnect

Based on the derivation in section 4.2, one would expect that utilizing multiple columns is beneficial. However, the above derivation does not take into account the manufacturability of the compliant interconnect design. Utilizing multiple columns would imply interconnects having a high aspect ratio. The higher the aspect ratio the more difficult it is to fabricate the interconnect. Hence, to compare the single column to the multiple columns it would be appropriate to assume the same aspect ratio. This is valid for fine pitch interconnects where the height of the interconnect is not a constraint (for

interconnects at a coarser pitch (>500μm) the height of the interconnects could be a concern). For a single circular column with a height H, a cross-section area A and a diameter D, the resistance, R_s would be

$$R_s = K\frac{H}{A} = K\frac{4H}{\Pi D^2} \qquad \textbf{(4.9)}$$

and the compliance, using Eq. 4.2, would be

$$C_s = K'\frac{H^3}{I} = 64K'\frac{H^3}{D^4} \qquad \textbf{(4.10)}$$

For the case of n multiple circular columns, each having a height h, a cross-section area a and a diameter d, the resistance for an individual column is

$$R'_m = k\frac{h}{a} = k\frac{4h}{\Pi d^2} \qquad \textbf{(4.11)}$$

And the compliance, using Eq. 4.2, would be

$$C'_m = K'\frac{h^3}{I} = 64K'\frac{h^3}{d^4} \qquad \textbf{(4.12)}$$

Considering the multiple columns collectively, the combined resistance is

$$R_m = k\frac{4h}{n\Pi d^2} \qquad \textbf{(4.13)}$$

And the compliance is

$$C_m = 64K'\frac{h^4}{nd^4} \qquad \textbf{(4.14)}$$

Now if the aspect ratio $P=H/D$ is kept the same in both cases, we get

$$R_s = K\frac{4P}{\Pi D}, C_s = 64K'\frac{P^3}{D}, R_m = K\frac{4P}{n\Pi d}, C_m = 64K'\frac{P^3}{nD} \qquad \textbf{(4.15)}$$

To ensure a valid comparison, the resistance for the two cases is kept the same, which implies that

$$D = nd \qquad \textbf{(4.16)}$$

And therefore the compliance for both the cases is the same.

Hence, there is no benefit gained in terms of compliance by utilizing multiple columns. In addition, even for the same aspect ratio, multiple columns would be harder to fabricate because of their smaller dimensions. Multiple columns, due to their spacing between them, would also occupy a greater area. Finally, using Euler-Bernoulli beam

theory, it can be shown that the stresses introduced in the interconnect for multiple columns is greater (for the same aspect ratio). In conclusion, as a consequence of the constraints imposed by manufacturability, to utilize the multiple path concept, the multiple electrical paths must lie in the in-plane direction rather than the out-of-plane direction and it is hence not feasible to utilize the multiple copper column approach for fine pitch interconnects.

4.5 Single-Path FlexConnect

Before implementing the multiple electrical path concept to develop a compliant interconnect design, a baseline single-path interconnect design is developed. The interconnect design is referred to as the single-path FlexConnect. The choice of this design is based on the results described in [Zhu 2003] where it shown that a semicircular arcuate beam without sharp corners gives good compliance in all three orthogonal directions. Schematic representations of the single-path FlexConnect design for interconnects at a 100μm pitch are shown in Figure 4.3a and Figure 4.3b. A horizontal arcuate structure is employed which connects to the die pads through a vertical anchor structure. The arcuate structure provides most of the compliance. The end of the arcuate beam has a circular pad. This is used during chip assembly, to provide a surface for the solder to wet the arcuate beam. Also, a neck is designed in the transition region from the circular pad to the arcuate structure. This ensures that due to surface tension effects, the solder would wet only the circular pad and not the remaining arcuate structure. This is because the planar dimensions of the circular pad are larger than that of the neck. Hence, to minimize the surface energy during reflow, the volume of solder and consequently the thickness of the solder will be greater on the circular pad as compared to the neck. Therefore, due to the presence of the neck, it is energetically not favorable for the solder to wet the arcuate beam. Solder should not wet the remaining arcuate structure, as this would detrimentally impact the compliance of the interconnect structure. A similar concept has been utilized previously for wafer-level packaging and is described in [Rinne

et al. 2000]. An experiment is conducted to verify this and is described in Chapter 7 of this dissertation.

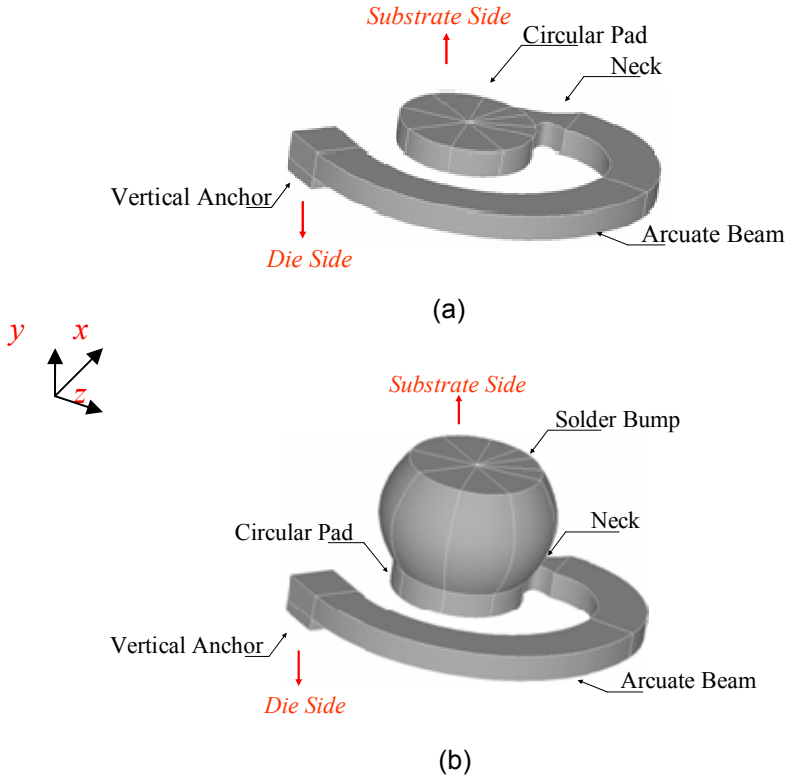


Figure 4.3: Schematic Representation of Single-path FlexConnect Design

Figure 4.3a represents the interconnect with a circular pad. In this case, for the purpose of chip-to-substrate assembly, solder paste is deposited on the substrate pads and the chip with compliant interconnects is then assembled onto the substrate through a reflow process. Figure 4.3b represents an alternate assembly scheme in which the solder is electroplated on the interconnect pads, and the chip with the interconnects is assembled on the substrate with or without solder paste on the substrate pads.

Copper is utilized as the interconnect material. This is because copper has low electrical resistivity which results in improved power distribution and device performance as well as reduced cross talk. Copper also has good electromigration properties. It is also cheap and easy to electroplate [Zhu et al. 2004].

4.6 Single-Path FlexConnect Design Characterization

The mechanical performance of the interconnects is characterized in terms of the diagonal compliance $c_d = ((c_x^2+c_z^2)/2)^{0.5}$, where c_x and c_z are the compliances in the in-plane direction as shown in Figure 4.3. The diagonal compliance is a composite metric which represents the in-plane compliance of the interconnect by a single number. It is the vector sum of the compliance of the interconnect in two orthogonal in-plane directions. Alternatively it can be interpreted as an engineering approximation of the compliance of the interconnect along a line which is at an angle of 45 degrees with respect to the *x* and *z* axis. For the case of FlexConnects the maximum in-plane compliance is observed along the *z* axis and the minimum compliance is observed along the *x* axis. The diagonal compliance lies between these two values.

To determine the diagonal compliance, the single-path Flexconnects are modeled in ANSYS using solid elements. The interconnects are modeled with a linear elastic material model with properties corresponding to copper. The elastic modulus is taken as 121 GPa and the Poissons ratio as 0.34.

Loading conditions correspond to completely constraining one end of the interconnect. In-plane displacements are imposed on the nodes at the other end of the interconnect. The resulting reaction forces are obtained and the compliance calculated as the ratio of the applied displacement to force.

The electrical performance is qualitatively described in terms of the resistance and self-inductance of the interconnects. The resistance and self-inductance of the interconnects are determined through numerical simulations in FastHenry. The resistivity of copper is taken as 1.772×10^{-6} Ω-cm. Two terminals are defined for the interconnect, one at either end of the interconnect.

The electrical and mechanical performance characteristics of the single-path FlexConnect design are determined and the results are summarized in Table 4.1.

As seen the single-path FlexConnect design has good electrical characteristics. However, due its low stand-off height, the mechanical compliance is significantly lower than the target compliance value of 7mm/N recommended by industry experts [Intel-Corporation 2001]. The low stand-off height is a consequence of the constraints imposed by the fabrication process utilized to fabricate FlexConnects (described in Chapter 5). Hence the single-path FlexConnect design needs to be improved to increase its compliance. This is achieved by utilizing the multiple electrical path concept and is described in the following section.

Table 4.1: Electrical and Mechanical Characteristics of Single-Path FlexConnect

	C_x (mm/N)	C_z (mm/N)	C_d (mm/N)	R_{DC} (mΩ)	L_{self} (pH)
Single-Path FlexConnects	0.53	1.03	0.82	31.48	58.8

4.7 Parallel-Path FlexConnects Design

As the mechanical compliance of the single-path FlexConnects is low, a parallel-path FlexConnect design is developed using the concept presented in Section 4.3. A schematic representation of the new parallel-path FlexConnect is shown in Figure 4.4. As discussed earlier, the compliant interconnect design is based on the work presented in [Zhu 2003].

Starting with the vertical anchor structure, two horizontal arcuate structures are fabricated. The ends of the arcuate beam meet at a circular pad, as shown in Figure 4.4. The transition from the relatively thin arcuate beam to the larger circular pad would serve the purpose of the 'neck' shown in Figure 4.3a and Figure 4.3b, limiting the solder to the circular pad. The thickness of the arcuate beam of the parallel-path FlexConnect is same as that of the single-path FlexConnect design shown in Figure 4.3. However, the width of each individual beam of the parallel-path FlexConnect is one-third that of the single-path

FlexConnect design. Also the curvature of the arcuate structure is modified to accommodate the 100µm pitch requirement. Fabrication of these interconnects is discussed in Chapter 5.

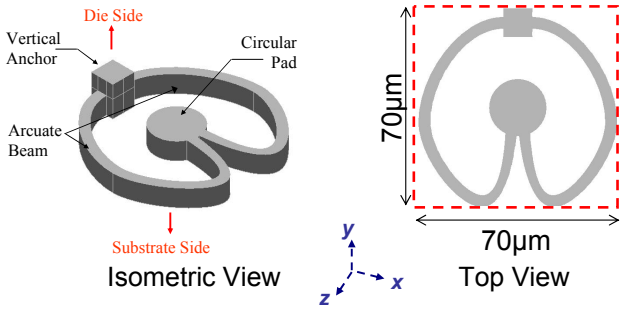


Figure 4.4: Schematic of parallel-path FlexConnect

Table 4.2: Electrical and Mechanical Characteristics of Parallel-Path FlexConnects

	C_x (mm/N)	C_z (mm/N)	C_d (mm/N)	R_{DC} (mΩ)	L_{self} (pH)
Single-Path FlexConnects	0.53	1.03	0.82	31.48	58.8
Parallel-Path FlexConnects	2.15	6.47	4.82	40.94	36.5

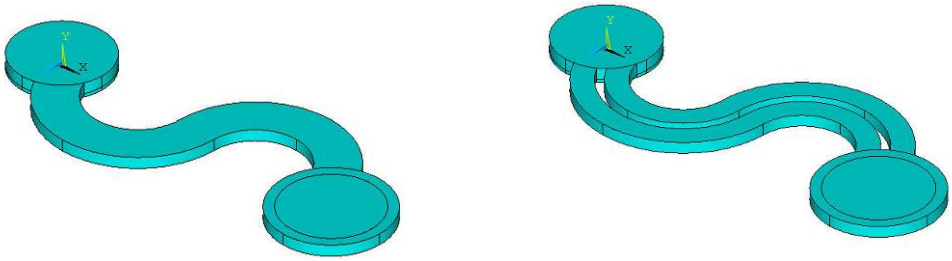
The mechanical compliance and the electrical parasitics of the parallel-path FlexConnects design are determined using the procedure discussed earlier. The results are summarized in Table 4.2. As seen, the inductance of parallel-path FlexConnects is lower than the single-path FlexConnects (-38%). The parallel-path FlexConnects has an in-plane compliance that is nearly six times (+488%) that of the single-path FlexConnects design. This compliance value is comparable to the target compliance of 7mm/N recommended by industry experts [Intel-Corporation 2001]. In other words, by using parallel electrical paths the compliance is increased and at the same time the inductance is

decreased, clearly illustrating the advantage of using the multiple electrical path approach. The reduction in inductance can be partly attributed to the magnetic flux of the two arcuate beams canceling each other, as they both have current flowing in the same direction. The compliance in the *x* direction presented in Table 4.2 for parallel-path FlexConnect was obtained by applying a negative (compressive) displacement along the *x* direction. The compliance was also determined by applying a positive (tensile) displacement along the *x* direction and was found to be equal to 2.13 mm/N, similar to the compliance determined through the compressive displacement. Similar simulations were not run for the compliance in the *z* direction as the interconnect is symmetrical about the *x* axis.

4.8 Extendibility to other Compliant Interconnects: Sea of Leads as an Illustrative Example

To demonstrate the generic nature of this concept of utilizing multiple electrical paths, the Sea of Leads (SoL) interconnect (Figure 2.10) is considered and the concept applied to it. Figure 4.5a shows the original geometry of the SoL interconnects. Figure 4.5b shows the modified geometry with the beam connecting the two pads being split into two halves, with the net cross-sectional area being kept the same as in Figure 4.5a. As the geometry and dimensions of the interconnect shown in Figure 4.5b are the same as that shown in Figure 4.5a, we would expect the resistance and inductance of the interconnect to remain about the same. If anything, the resistance at high frequencies for the interconnect shown in Figure 4.5b will lower than that of the interconnect shown in Figure 4.5a. This would be due to the increased surface area which is significant when the skin-effect starts becoming prominent at higher frequencies. Through a similar procedure as described above and considering the interconnects to be fabricated out of copper, the compliance of the interconnects shown in Figure 4.5a and Figure 4.5b, are calculated in the in-plane directions *x* and *z*. The results are shown in Table 4.3. As seen,

by utilizing the multiple electrical path concept a substantial increase in in-plane compliance is obtained, with the diagonal compliance increasing by 240%. The electrical parasitics for both the cases would be the same. In other words, the multiple electrical path design concept is easily extended to other compliant interconnects and results in an increase in the mechanical performance of the interconnects without compromising on the electrical performance.



(a) (b)

Figure 4.5: SoL Interconnects (a) Single-Path (b) Parallel-Path

Table 4.3: Sea of Leads Compliance

	Cx **(mm/N)**	***Cz*** **(mm/N)**	***Cd*** **(mm/N)**
Single-Path Sea of Leads	0.45	0.91	0.72
Parallel-Path Sea of Leads	1.61	3.06	2.45

4.9 Modeling of Electrical Performance of Parallel-Path FlexConnects

A more detailed modeling of the electrical performance of parallel-path FlexConnects is presented in this section.

4.9.1 High-Frequency Modeling

As the off-chip interconnects would carry high-frequency signals, it is important to characterize the parasitics of the interconnects at such frequencies. At high frequencies

the phenomenon of skin-effect is observed which results in crowding of the current around the surface of the conductor, increasing the AC resistance of the conductor. The resistance and self-inductance of parallel-path FlexConnects as a function of frequency are determined through numerical simulations in FastHenry. Material properties are kept the same as before. The simulations are run from a frequency of 10Hz to a frequency of a 100 GHz. The results are shown in Figure 4.6.

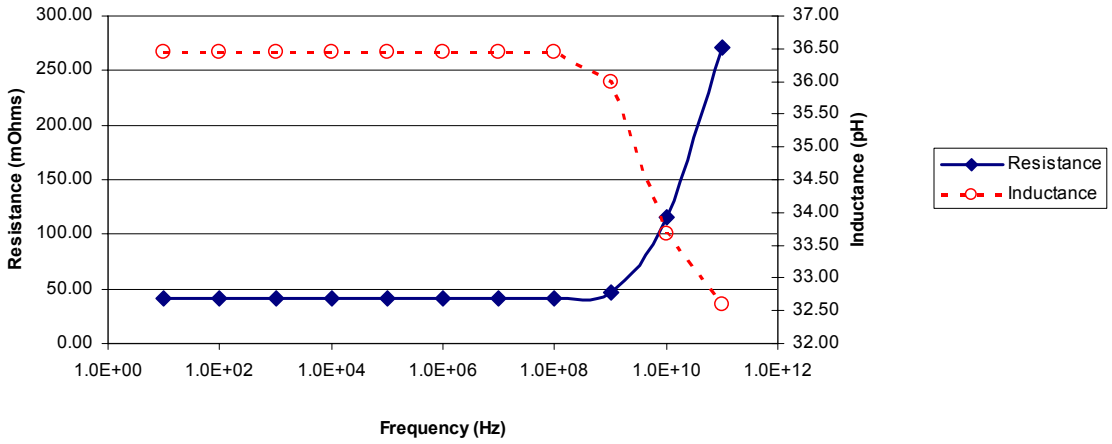


Figure 4.6: Inductance and Resistance of Parallel-Path FlexConnect as a Function of Frequency

As seen, there is a significant increase in the resistance due to the "skin-effect" as one goes above 1GHz. The inductance of the parallel-path FlexConnect is seen to decrease below 100MHz.

4.9.2 Trace Orientation Impact on Interconnect Resistance

Another concern with the parallel-path FlexConnect is that the orientation of the trace supplying the current to the interconnect may impact the interconnect resistance. It is conceivable that if the traces to and from the interconnect are not symmetrical with regards to the interconnect, more current may flow in one electrical path rather than the other. Such "Current Crowding" or non-homogenous distribution of current density

within the interconnect may result in the formation of localized hot-spots, increase the overall resistance of the interconnect and accelerating electromigration.

To study this, simulations are created in FastHenry to determine the combined resistance of the interconnect and the trace. The resistance is determined for different trace orientations as a function of frequency. The different trace orientations considered are shown in Figure 4.7. The results obtained are shown in Figure 4.8.

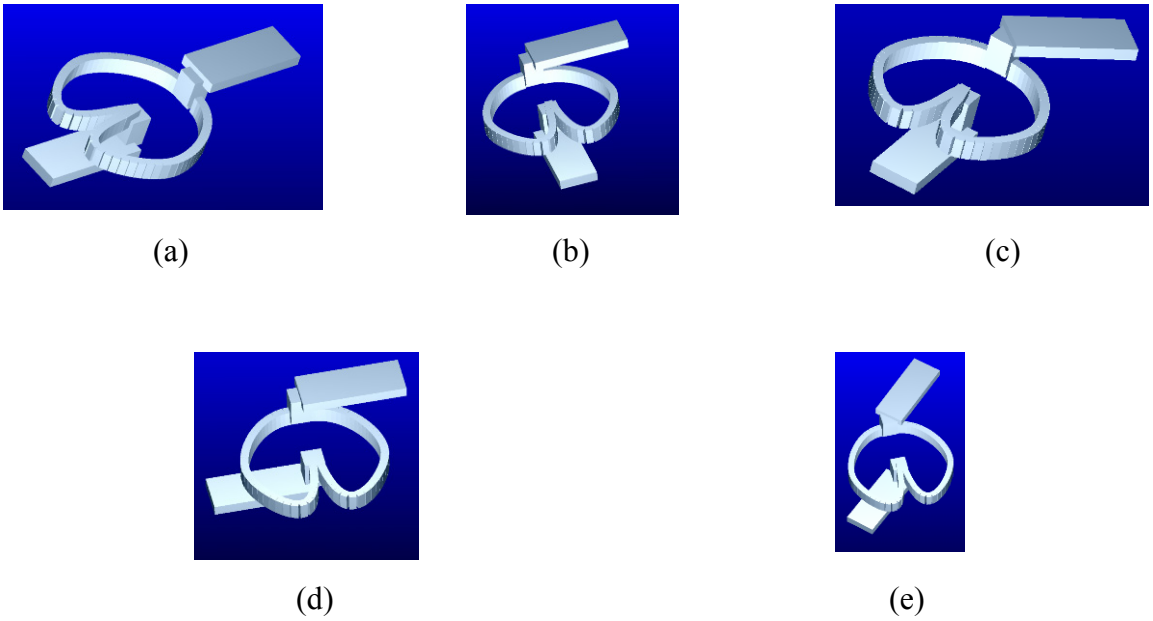


Figure 4.7: Lead Orientation with respect to Interconnect for FastHenry Simulations (a) both traces at '0' deg (b) one trace at '0' deg, second trace at '90' deg (c) one trace at '0' deg, second trace at '45' deg (d) both traces at '90' deg (e) both traces at '45' deg

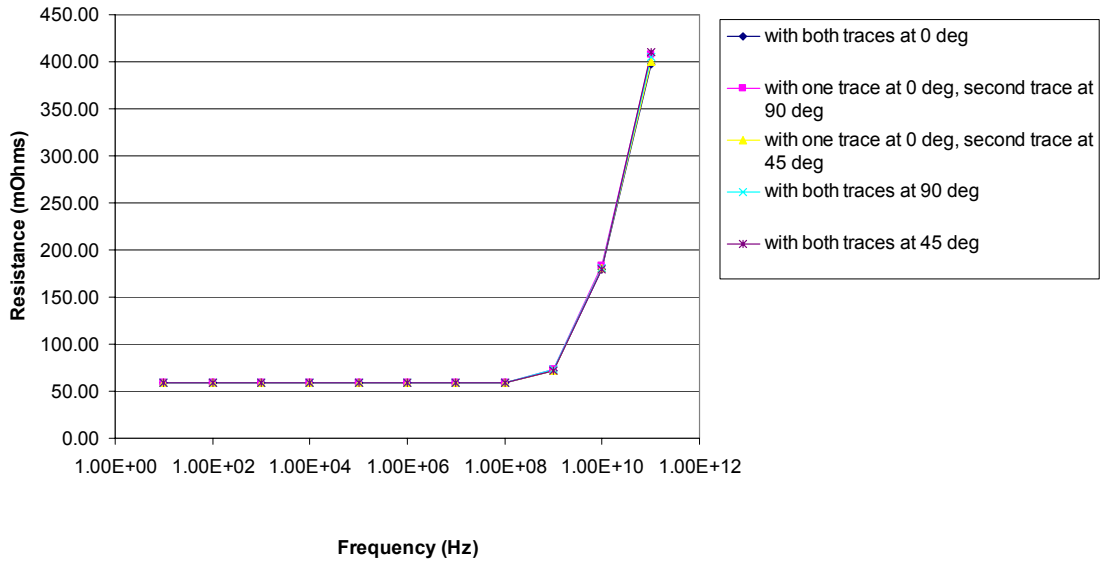


Figure 4.8: Resistance as a Function of Frequency for Different Trace Orientations

As can be seen, the combined resistance of the interconnect and the trace is independent of the orientation of the trace. To further investigate this, models are created in ANSYS to determine local current densities. Only DC resistance is obtained from the simulations run using ANSYS. ANSYS is utilized as FastHenry does not provide local current densities. The various geometries analyzed are shown in Figure 4.9. The properties of copper are kept the same as before. A voltage of 1V is applied to one end while the other end is kept at 0V. Plot of the current densities for two cases are shown in Figure 4.10. Similar plots are obtained for the remaining two cases. For all cases, the maximum current density in the interconnect is the same. In addition, the contour plots for current density are also seen to be similar. This again indicates that the orientation of the trace does not result in a non-homogenous current distribution.

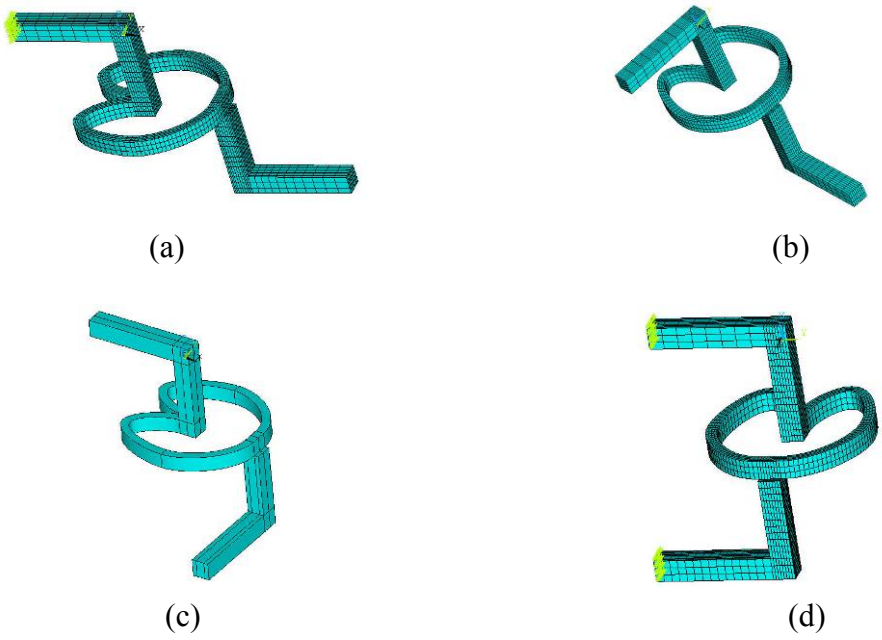
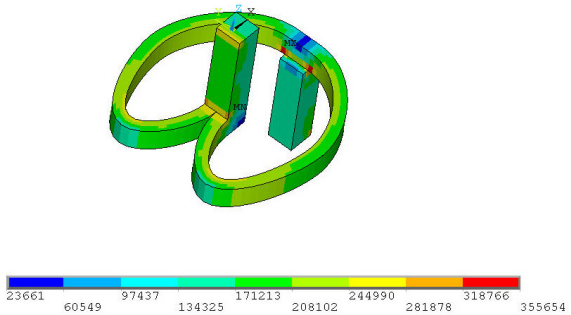
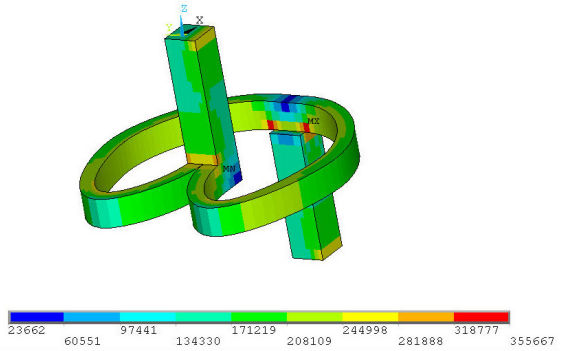


Figure 4.9: Lead Orientation with respect to Interconnect for ANSYS Simulations (a) both traces at '0' deg (b) one trace at '0' deg, second trace at '90' deg (c) one trace at '90' deg, second trace at '0' deg (d) both traces at '90' deg



(a)



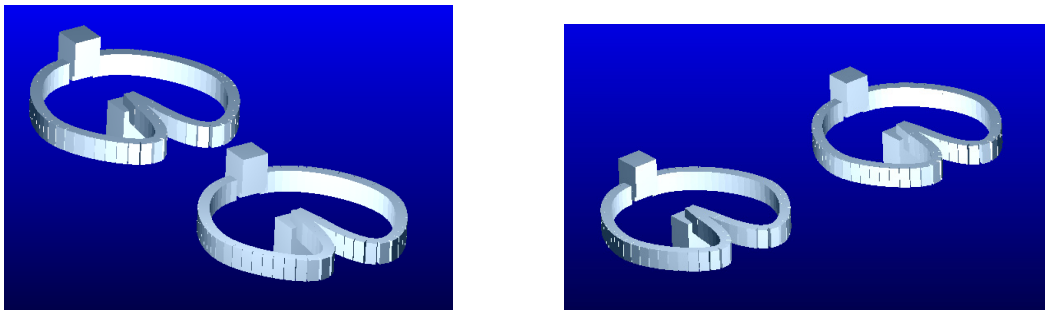
(b)

Figure 4.10: Current Density in Interconnect for (a) both traces at '0' deg (b) one trace at '0' deg, second trace at '90' deg

4.9.3 Mutual Inductance of FlexConnects

Apart from the self-inductance of the interconnect, it is also important to investigate the mutual inductance between neighboring interconnects. The mutual inductance contributes to cross-talk. Mutual inductance can also have a subtractive or additive contribution to the loop inductance of a pair of interconnects between a set of driver and receiver circuits. For this purpose interconnects in two configurations are studied and are show in Figure 4.11. For both cases interconnects at a 100µm pitch are considered. For the first case (Figure 4.11a) the mutual inductance between the interconnects is found to be 1.50pH and for the second case (Figure 4.11b) the mutual

inductance between the interconnects is found to be 2.02pH. In both cases the mutual inductance is minimal. The mutual inductance is again determined using FastHenry.



(a) (b)

Figure 4.11: Configuration of Interconnects Studied to Determine Mutual Inductance of FlexConnects

4.9.4 Capacitance of FlexConnects

In general, it is difficult to accurately evaluate the capacitance of an off-chip interconnect as this depends upon other components of the electronic package like the location of traces and ground planes. Keeping this in mind, certain configurations are chosen with an intention of developing an understanding of the capacitance of parallel-path FlexConnects rather than accurately calculating the capacitance of the interconnect when it is used in an electronic package.

The capacitances are determined using FastCap. The configurations studied are shown in Figure 4.12. As the parallel-path interconnects are free-standing, the dielectric medium is taken as air with a relative permittivity of 1. Figure 4.12a shows a single interconnect, whose self-capacitance is calculated to be 2.851fF. Figure 4.12b shows a single interconnect at a distance of 1μm from the surface of a conducting plane of dimensions 200μm x 200μm. If the interconnect is taken as conductor 1 and the conducting plane is taken as conductor 2, the following capacitance matrix is obtained

$$C_{11} = 7.559\,fF; C_{12} = C_{21} = -7.039\,fF; C_{22} = 14.68\,fF$$

For the configurations shown in Figure 4.12c and Figure 4.12d a pair of interconnects at a 100μm pitch are considered. For the configuration shown in Figure 4.12c the following capacitance matrix is obtained

$$C_{11} = C_{22} = 3.115\,fF; C_{12} = C_{21} = -0.8658\,fF$$

For the configuration shown in Figure 4.12d the following capacitance matrix is obtained

$$C_{11} = C_{22} = 3.108\,fF; C_{12} = C_{21} = -0.8481\,fF$$

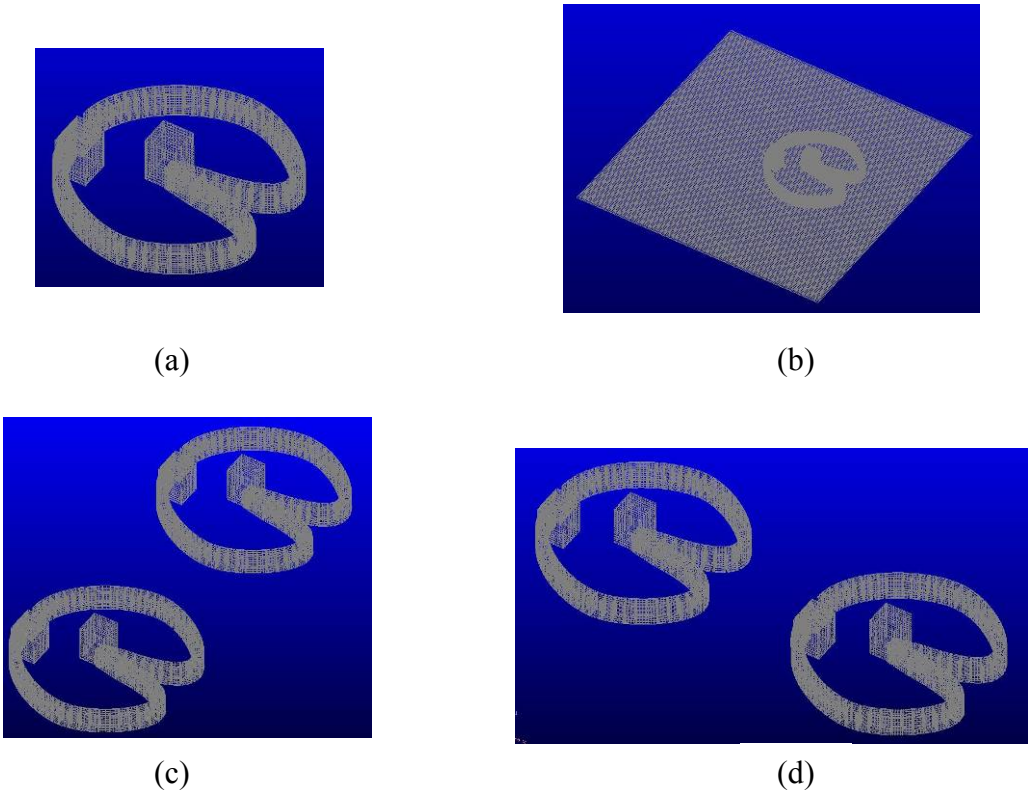


Figure 4.12: Configurations Studied for Capacitance Calculation

The results obtained are along expected lines. The maximum capacitance values are obtained for the configuration shown in Figure 4.12b, as a ground plane is present with a large surface area. More importantly, as expected, all the cases studied indicate a low value for the capacitance of the interconnects. In conclusion, even though the configurations are not an accurate representation of an actual electronic package, the low

values of capacitance obtained would indicate that capacitance of a compliant interconnect is not much of a concern.

4.10 Conclusion

In this chapter, a design concept is proposed which involves utilizing multiple electrical paths as part of the compliant interconnect design. An analytical model is developed to show that such an approach allows for an improvement in electrical performance without compromising on mechanical performance. In addition, utilizing multiple electrical paths also results in a redundant design, allowing the interconnect to continue functioning even if one of the electrical path fails. Using multiple columns as a single interconnect is then discussed and it is shown that at a fine pitch it is not recommended to replace a single column by multiple columns. Hence, the multiple electrical paths must lie in the in-plane direction and not in the out-of-plane direction. A new compliant interconnect called FlexConnects is then developed. Using numerical models the parallel-path FlexConnect is compared against a single-path FlexConnect. It is shown that the parallel-path FlexConnect has higher mechanical compliance than the single-path FlexConnect and reduced inductance. In other words, by utilizing multiple electrical paths, the mechanical performance and the electrical performance are increased at the same time. Significantly, the parallel-path FlexConnect is a compliant interconnect with a low value of inductance (36.5 pH). The generic nature of the multiple electrical path concept is shown by applying it to the case of the Sea of Leads interconnect. For the Sea of Leads interconnect when two interconnect paths are utilized, the electrical performance remains the same, but the in-plane mechanical compliance increases by 240%. Further modeling of the parallel-path FlexConnect is then performed. High frequency modeling of the inductance and resistance of the interconnect is performed. Skin-effect results in the resistance of the interconnect increasing after 1GHz. The inductance of the interconnect starts decreasing above 100 MHz. Through numerical simulations it is shown that the orientation of the trace feeding to and from the

interconnect does not affect the overall resistance of the interconnect and the maximum current density in the interconnect. The mutual inductance of parallel-path FlexConnects at a 100μm pitch is also determined and is seen to be minimal. The capacitance of parallel-path FlexConnects is also determined and is shown to be negligible.

CHAPTER 5
FABRICATION OF COMPLIANT INTERCONNECTS

5.1 Introduction

Although compliant interconnects offer several advantages over conventional solder bumps, unless they can be fabricated cost effectively and with high yield, their implementation will be limited. To meet these requirements it is preferable that the interconnects be fabricated in a batch manner. In addition, fabrication of compliant interconnects at an interconnect pitch of a 100μm requires the definition of features at the micron scale. Similar requirements are imposed on MEMS devices and hence it would be suitable to utilize a MEMS based fabrication technique to realize compliant interconnects. Such a fabrication process is developed in this chapter with the intention of realizing free-standing compliant interconnects which have high fabrication yield, are uniform across the wafer and are cost-effective at the same time. The design of the compliant interconnects fabricated correspond to that of the parallel-path FlexConnect described in Chapter 4.

In this chapter, a conceptual description of the fabrication process is discussed (Section 5.2). This is followed by a description of the photoresists utilized (Section 5.3). A fabrication process to realize the parallel-path FlexConnects is then proposed (Section 5.4). A description of the test vehicle design used for the fabrication process is then provided (Section 5.5). This is followed by a description of the process parameters and their influence on the fabrication process (Section 5.6). Finally, results from the fabrication process are presented (Section 5.7).

5.2 Conceptual Description of Fabrication Process

A cost effective fabrication technique should realize a compliant structure with a minimum number of processing steps, preferably utilizing conventional semiconductor processes. Also, batch fabrication of interconnects would be necessary to realize cost

efficiency. Fabricating the interconnects at the wafer level using photolithography enabled batch processing would satisfy the above criteria. The photoresist would be patterned using lithography to define molds in the shape of the compliant interconnect. The compliant interconnect material can then be plated into the mold. The photoresist can then be stripped to realize the free-standing compliant interconnect.

In general, for an interconnect to be compliant it must be able to deform freely. Hence, the part of the compliant interconnect which provides compliance needs a standoff from the surface of the silicon and the surface of the substrate. To produce the standoff from the die a sacrificial layer could be utilized. Such an approach is extensively used in the fabrication of MEMS devices. A compliant interconnect fabricated in this manner is very similar to a MEMS structure as it is a mechanical device that undergoes deformation. Such an approach has been implemented for the G-Helix and SoL compliant interconnects [Zhu et al. 2004; Dang et al. 2006]. However, in both cases, one masking step is used to provide the standoff and subsequent masking steps are used to define the remaining interconnect geometry. However, the photoresist used to define openings in the chip passivation could also be utilized to provide the standoff for the compliant interconnect. In this manner one masking step is eliminated. Using this concept along with photolithography enabled batch processing a more cost effective fabrication process for compliant interconnects can be developed which utilizes a single masking step in addition to the masking step used to define openings in the passivation layer. Solder can be utilized to attach the interconnect to the substrate, providing standoff from the substrate.

5.3 NR7-1500P and NR9-8000P Photoresists

For the purposes of fabricating the compliant interconnects NR7-1500P and NR9-8000P photoresists supplied by Futurrex Inc are utilized. Both photoresists are negative, polyhydroxy-styrene based photoresists designed for i-line applications. In addition, both photoresists have cyclohexanone as the principal solvent and utilize a TMAH based

developer. Advantages associated with these photoresists include short develop times, short bake times and easy removal using acetone. NR7-1500P has a temperature resistance of up to 180°C. NR9-8000P has a temperature resistance of up to 100°C. Hence, we would expect NR7-1500P to withstand processing at elevated temperatures and be more dimensionally stable when compared to NR9-8000P. On the other hand, NR9-8000P can be used to define thicker photoresist films. For example, at a coating spin speed of 3000rpm, NR9-8000P has a film thickness of around 8μm whereas at the same coating spin speed NR7-1500P has a film thickness of around 1.5μm.

5.4 Fabrication Process Overview

The concept described in Section 5.2 is used to develop a fabrication process for FlexConnects, which is shown in Figure 5.1. A brief description of the fabrication process is provided below and a more detailed discussion is provided in Section 5.6 of this chapter.

As seen in Figure 5.1, on a given integrated circuit wafer with die pads (Figure 5.1a) a dielectric passivation layer is deposited (Figure 5.1b). This is followed by depositing and patterning a photosensitive layer to define openings in the passivation layer (Figure 5.1c). A Ti/Cu/Ti seed metal layer is then deposited to facilitate the deposition of copper for the interconnect structure (Figure 5.1d). A second photosensitive layer is then deposited and patterned to define the arcuate structure, and the circular pad for solder (Figure 5.1e). Copper is then electroplated, filling up the pattern defined both by the first and second photosensitive layer (Figure 5.1f). In this manner, the bottom anchoring structure (alternatively referred to as the vertical post), the arcuate structure, and circular pad structure are fabricated in a single step. For the purpose of assembly using solder suitable interface metallurgies are deposited on the top surface of the arcuate beam (Figure 5.1g). The interconnect structure is then released by etching and/or stripping the photosensitive layers and the seed layers (Figure 5.1h). In this manner, the free-standing compliant interconnect (parallel-path FlexConnect) structure illustrated in

Figure 4.4 can be realized. This fabricated interconnect is assembled using solder present on the surface of the board.

An alternate method to assemble the interconnect would be by plating solder on it. This would result in a parallel-path version of the structure described in Figure 4.3b. To realize this design, steps described in Figure 5.1a to Figure 5.1f are repeated. The remaining steps are described as follows. After step Figure 5.1f, a third photosensitive layer can be deposited and patterned to define an opening in the shape of the circular pad (Figure 5.1j). Suitable interface metallurgies (e.g. Ni) for the purpose of assembly using solder can then be deposited on the top surface of the circular pad. This is followed by electroplating solder into the mold defined by the photoresist (Figure 5.1k). The interconnect structure is then released by etching and/or stripping the photosensitive layers and the seed layers. The solder is reflowed once the interconnect structure is released (Figure 5.1m). In this manner, the free-standing compliant interconnect structure illustrated in Figure 4.3b and its parallel-path analog can be realized. The interconnects are batch fabricated on a single wafer. Once the interconnects have been fabricated, the wafer is singulated into individual dies.

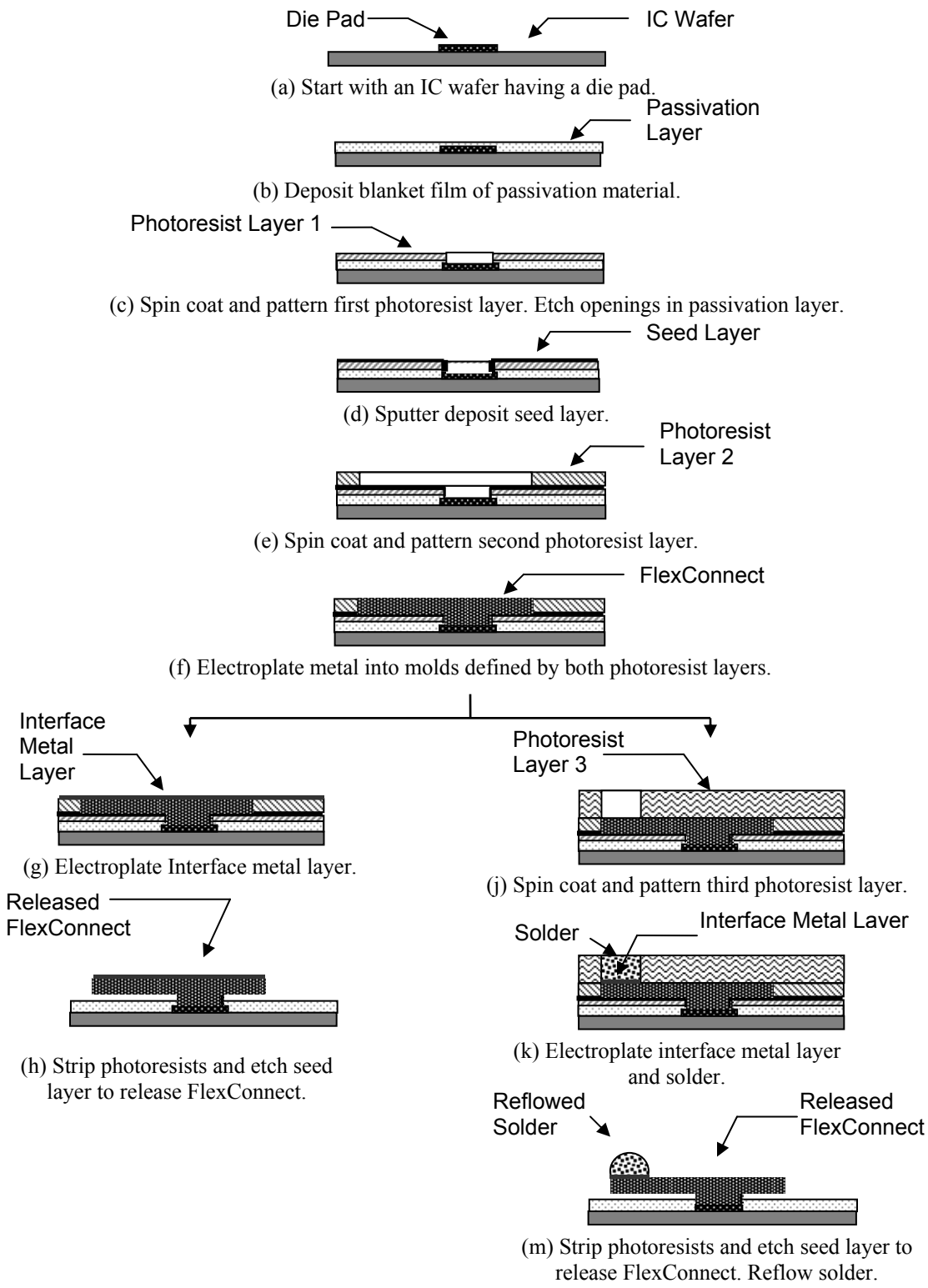


Figure 5.1: Fabrication Process for FlexConnects

5.5 Fabrication Process Test Vehicle Design

The interconnects are fabricated on 4 inch Silicon wafers. The die size is 20mm x 20mm. Consequently, a maximum of twelve dies could be accommodated on a single wafer. This is illustrated in Figure 5.2. The blue line marks the outline of the 4 inch wafer and the green lines mark the outline of the individual dies. One of the die locations is not utilized (marked by a red cross) and hence a maximum of eleven individual dies can be obtained from each wafer. To mimic the presence of the die pads a blanket Ti/Cu/Ti seed layer is deposited. This seed layer could be patterned; however this would not influence the ability to fabricate the interconnect and would require an additional mask. Hence, the seed layer is not patterned, eliminating the need for an additional mask. Subsequent to the deposition of the seed layer, the steps described in Figure 5.1 are performed to fabricate the interconnects.

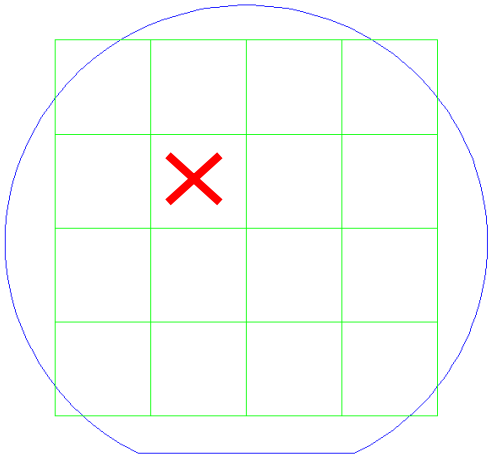


Figure 5.2: Individual Die Outlines for a Single 4" Wafer

The mask design for an individual die is shown in Figure 5.3. For the purposes of providing a visual aid during the dicing of the wafer, each individual die has a line (marked in yellow in Figure 5.3 and referred to as dicing saw line) along its periphery as part of the first mask layer. Alignment marks (Figure 5.4b and Figure 5.5b) are present at the bottom left corner and the top right corner for the purposes of alignment during the

fabrication process. These alignment marks can also be used during the assembly of the interconnects. Each individual die has three rows of interconnects at a 100µm pitch along the periphery, resulting in a total of 2364 interconnects per die. The choice of this layout is dictated by the substrates available for the assembly of these interconnects. As the substrates available had such a three-row peripheral array of substrate, a similar design had to be adopted for the masks utilized to fabricate the interconnects. If needed, the interconnects can be easily fabricated in a full area array configuration at a 100µm pitch (40,000 interconnects for a die size of 20mm X 20mm).

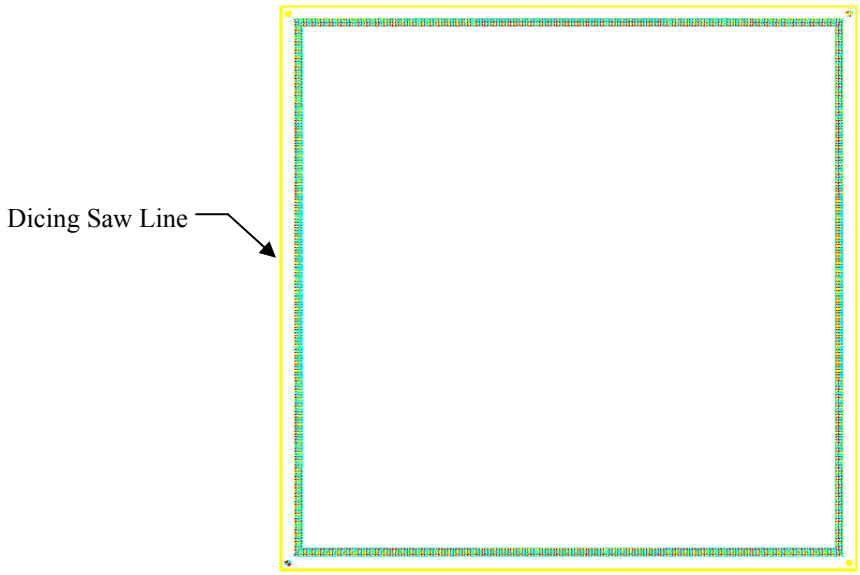


Figure 5.3: Mask Layout for Individual Die

To realize the design shown in Figure 4.4, two masking steps are required. The first masking step is used to define an opening in the passivation layer and hence only one additional masking step is required to fabricate the compliant interconnect. If solder is to be plated on the interconnect (Figure 5.1j to Figure 5.1m), a third masking step (second additional masking step) is required. Figure 5.4 shows the mask design with the first two masking layers. Figure 5.5 shows the mask design with three masking layers. The first mask layer is shown in yellow, the second mask layer (overlaid above the first

mask layer) is shown in cyan, and the third mask layer (overlaid above the first and second mask layer) is shown in red.

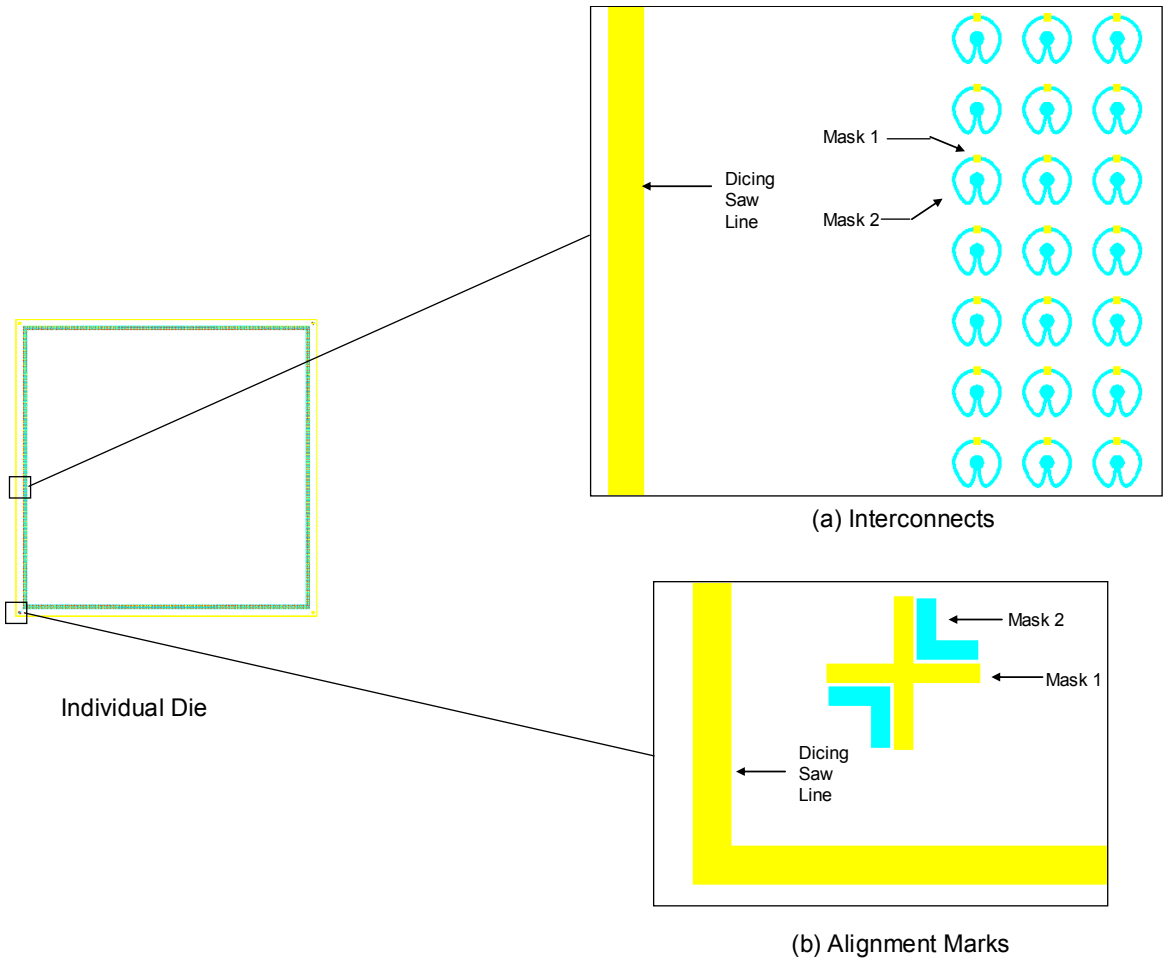


Figure 5.4: Mask Layout Depicting First Two Layers

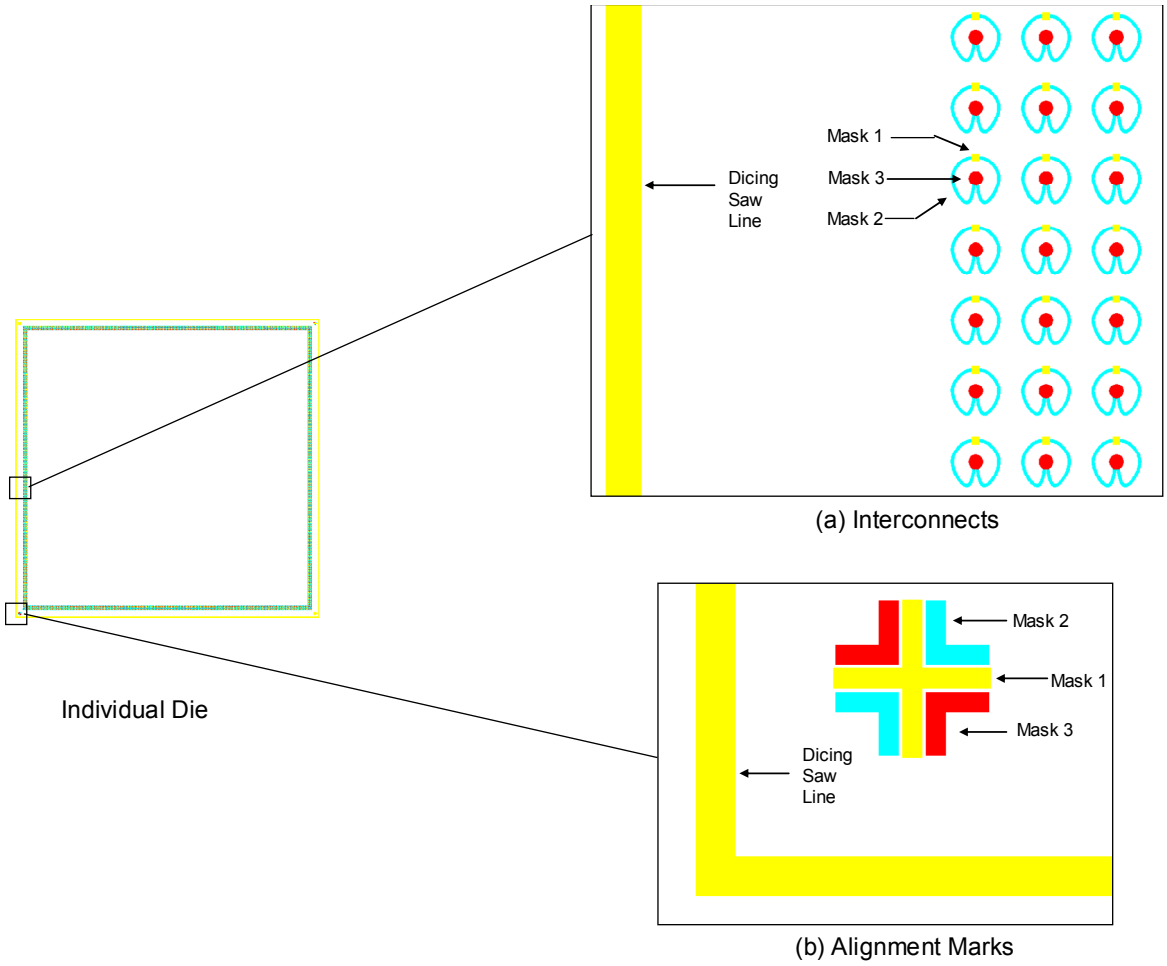


Figure 5.5: Mask Layout Depicting All Three Layers

In addition, the orientation of the interconnects is varied across a single die. The reasons for doing this are a result of compliant interconnects not being rotationally symmetric like solder joints. Consequently the in-plane compliance of the interconnects differs depending upon the direction in which the displacement is applied. Ideally we would like the interconnects to experience a displacement in a direction in which their compliance is greatest. For a die assembled on a substrate the center of the die represents the neutral point i.e. the point at which the die does not move relative to the substrate when a thermal load is applied. A line drawn from the center of the die to the compliant interconnect is the direction in which the compliant interconnect deforms. It is hence desirable to orient the interconnect in such a manner that this line is in the direction in

which the interconnect compliance is the greatest. Therefore, as illustrated in Figure 5.6, the interconnect has three different orientations depending upon its location in the die. Such an approach allows maximal use of the interconnect compliance.

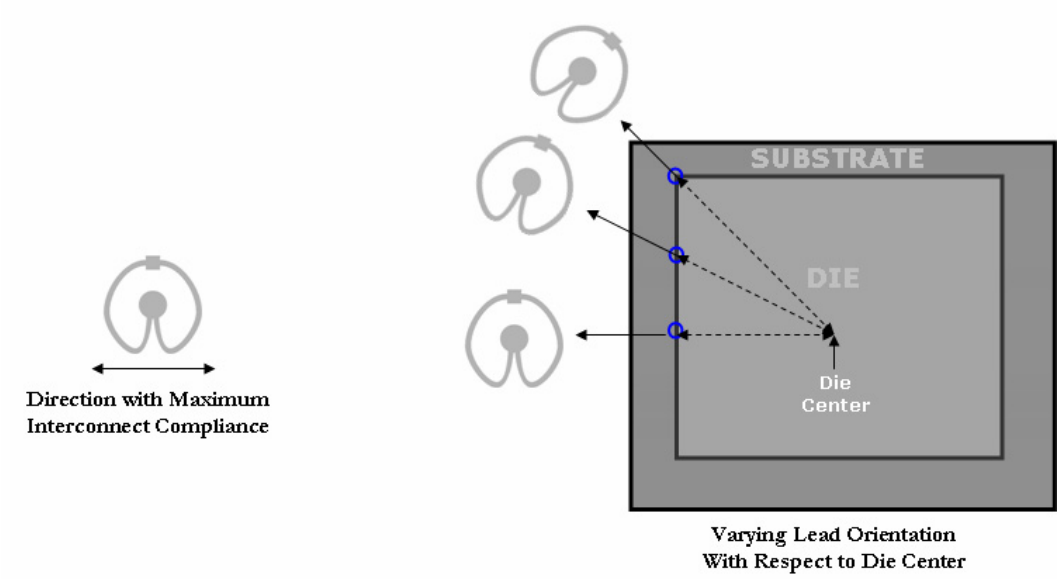


Figure 5.6: Variation of Compliant Interconnect Orientation

5.6 Process Parameters for Fabrication of FlexConnect

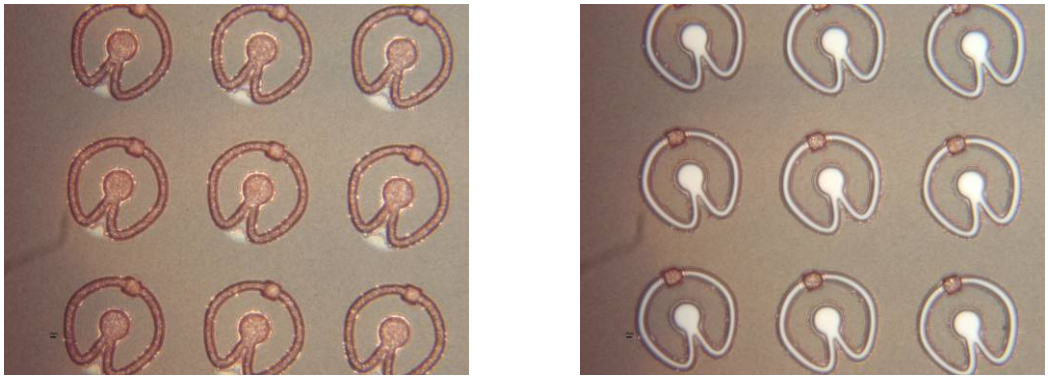
Before initiating fabrication, the wafer is sequentially rinsed with acetone, methanol, isopropanol, and DI water. The wafer is then dried using an air gun supplied with Nitrogen and put in an oven set at 110°C for 10 minutes to dehydrate the wafer. In the following description of the fabrication process, the above procedure will be referred to as an AMI clean process. Next, the seed layer (Ti/Cu/Ti – 30nm/100nm/30nm) to mimic the die pad is deposited. The initial seed layer of Ti provides adhesion, the Cu seed layer provides an electrically conductive layer, and the final Ti layer acts as a visual aid to determine when the passivation layer is etched, exposing the Cu seed (the translucent SiO_2 passivation layer is etched by Buffered Oxide Etch (BOE - 6 parts 40% NH_4F and 1 part 49% HF), which etches Ti as well). An AMI clean process is then performed. The fabrication process described from Figure 5.1a to Figure 5.1h are then followed.

5.6.1 Passivation Layer Deposition

The next step is the deposition of a blanket passivation layer, as shown in Figure 5.1b. Examples of passivation layer materials include SiO_2, SiN, and polyimide. In this work, SiO_2 is PECVD deposited as the passivation layer. A Plasma-Therm PECVD machine is utilized with deposition done at a temperature of 250°C, pressure of 900mTorr, and power of 25W. The gas configuration is SiH_4 (2% in N_2) at 400 sccm and N_2O at 900 sccm. SCCM stands for standard cm^3/min. The approximate deposition rate is 40nm/min.

The thickness of the $Si0_2$ layer is observed to impact the fabrication process. A thin SiO_2 layer (less than 1μm) is seen to result in low yield on interconnect fabrication. This is because a thinner layer of SiO_2 results in poor adhesion of the interconnect to the silicon substrate. However, when the thickness of the SiO_2 layer is increased, the electroplating step (Figure 5.1f) had problems. It is observed that certain dies would not have any metal plated in the arcuate beam regions. More specifically, two scenarios are observed. As shown in Figure 5.7, either all the arcuate beams for a particular die are electroplated (Figure 5.7a) or none of the arcuate beams for a particular die are electroplated (Figure 5.7b). In addition, the dies where electroplating is observed, are more likely to be present towards the edge of the die. This is found to be caused by a combination of two factors – the mask design and undercutting of the passivation when openings are defined in the passivation. The first layer mask design has a dicing saw line around each individual die. As the electric current for the purpose of electroplating is supplied from one side of the wafer, it is necessary to ensure electrical continuity across the dicing saw line. Therefore the seed layer deposited must be continuous across this dicing saw line. If that is not the case for a particular die, then it is electrically isolated from the source of the electric current and hence the arcuate beams are not electroplated. The vertical posts are still electroplated due to current being supplied through the initial

seed layer. The reason that a die gets electrically isolated is because of the undercutting of the SiO_2 layer by the isotropic wet etch process. Due to the undercut, the sputter deposited seed layer may not be able to cover the sidewalls of the trench defined through the passivation layer by the dicing saw line. This introduces an electrical discontinuity. This is illustrated in Figure 5.8. The thicker the SiO_2 layer, the more is the etch time, the greater is the undercut and the more difficult it is for the seed layer to cover the sidewall. Hence, a thicker SiO_2 layer results in the arcuate beams of certain dies not being electroplated. Dies along the edge of the wafer are less likely to have this problem due to the sputtered seed layer covering the edge of the die, and hence providing an alternate electrical path. To correct this problem, thicker seed layers are attempted but are not seen to help. A thinner SiO_2 layer is also not an option due to reasons discussed above. One solution would be to modify the mask design such that the dicing saw line is not continuous around the die, thus ensuring electrical continuity for each die. However, this would require a redesign of the mask. Hence, alternatively the fabrication process is modified. After the step shown in Figure 5.1d, an additional electroplating step is introduced, filling the vertical post. This ensured electrical continuity through the bottom seed layer and resulted in plating being observed in all the arcuate beams. The additional electroplating step is not necessary and needs to be introduced as a result of a flaw in the mask design. Correcting for this flaw in the mask design would eliminate the additional electroplating step.



(a) (b)

Figure 5.7: Electroplating of Arcuate Beams

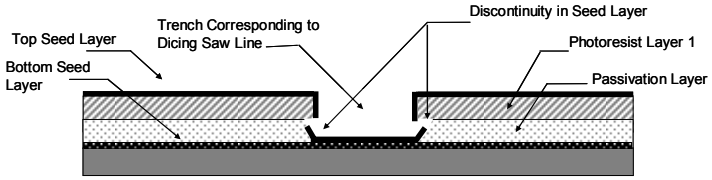


Figure 5.8: Undercut in SiO_2 Resulting in Seed Layer Discontinuity

Taking the above factors into consideration, a 2μm thick SiO_2 passivation layer is utilized. This corresponded to a deposition time of approximately 45 minutes. To minimize the formation of pin-holes, SiO_2 is deposited in three steps of 15 minutes each, with the wafer rotated after every step. After the passivation layer deposition, another AMI rinse is performed.

5.6.2 First Masking Step

The next step is the deposition and patterning of the first photoresist layer using the first layer mask (Figure 5.1c). NR7-1500P (supplied by Futurrex®) photoresist layer is used for this step. NR7-1500P is utilized because of its dimensional stability at high temperatures. This is important as a seed layer will be sputter deposited on this photoresist followed by a second layer of photoresist being spun on top of it. The data

sheet supplied by the manufacturer is used as a guide to determine the process parameters for the photoresist. The photoresist is spin coated on the silicon wafer, the spin speed is 800rpm with a ramp rate of 500rpm/sec and a spin time of 40secs, resulting in a photoresist layer that is approximately 2μm thick. This is followed by a pre-bake step in which the wafer is placed on a hot plate set at 150°C for 1 minute. The pre-bake step helps to drive the solvent out of the photoresist. Subsequently the wafer is placed in a mask aligner and the photoresist is exposed to UV light through the first layer mask. The mask aligner used is an EV620 mask aligner manufactured by the EV Group (EVG). This mask aligner has an intensity measured to be in the range of 9-11 mW/cm^2 at a wavelength of 365nm. A 17sec exposure time on the EV620 is found to be optimal. NR7-1500P is a negative photoresist, and the UV light helps to initiate the cross-linking of the photoresist. To complete the cross-linking process, a post-exposure bake is performed. As part of the post exposure bake, the wafer is placed on a hot plate set at 100°C for 1 minute. The next step involves the development of the photoresist. RD6, a TMAH based developer supplied by Futurrex®, is utilized. The wafer is immersed in the developer and the container with the developer is agitated by hand. A develop time of 15secs is found to be optimal. The develop process results in the photoresist not exposed to UV light being removed, realizing the molds used to define the vertical post. After the develop process is complete the wafer is rinsed in DI water and then dried using an air gun supplied with Nitrogen. This is followed by a hard bake step, with the wafer placed on a hot plate set at 100°C for 20 minutes. The hard bake step ensures that any residual solvent present in the photoresist is removed. After the hard bake step, a “descum” process is run in a Plasma-Therm Reactive Ion Etchant (RIE). The descum process removes any residual photoresist present in the openings defined by the photoresist and is require to ensure good yield on fabrication. The descum process is run for 1 minute. The recipe used in the RIE for dry etching NR7-1500p is as follows:

- RF Power: 300W

- Chamber Pressure: 280mTorr
- O_2 Flow Rate: 45 SCCM
- CHF_3 Flow Rate: 5 SCCM

The next step is the patterning of the passivation layer by etching it through the openings defined by the first layer photoresist. The etchant used is BOE, which also etches the top Ti layer of the bottom Ti/Cu/Ti seed layer. The end of the etching process is marked by the appearance of the golden-brown color of the Cu seed layer. To ensure a uniform etch, the wafer is taken out of the BOE solution every 30secs and rinsed with DI water. This minimizes the entrapment of air in the openings defined by the photoresist which could prevent the etching of the SiO_2 and Ti layers. The total time taken to etch a 2μm thick SiO_2 layer and 20nm thick Ti layer is found to be approximately 5 minutes.

As described in Section 5.6.1, the fabrication process described in Figure 5.1 is modified with an additional electroplating step introduced. For the purposes of initiating the electroplating process the copper seed layer previously deposited is utilized. Electroplating is an electrochemical process involving the deposition of a material on a conductive surface through the reduction of cations present in the electroplating solution. A typical electroplating setup used for plating copper into the molds defined by the photoresist is shown in Figure 5.9. As seen, there are four main components – the cathode, the anode, the current source and the electroplating solution. During the electroplating process DC current is supplied by the current source. A constant current source is utilized in this work. The negative terminal of the current source is connected to the cathode and the positive terminal of the current source is connected to the anode. The cathode corresponds to the material on which the copper is deposited, which in this case is the wafer. The anode is a copper source which acts as a consumable electrode, replenishing the copper in the electroplating solution. A copper clad FR4 board is used as a copper source. The electroplating solution has cations of the material to be deposited i.e. copper. Other chemicals are also present in the electroplating solution which aid in

the electroplating process. The electroplating solution is conductive, providing a conductive path between the anode and the cathode, and hence completing the circuit between the two terminals of the current source. The composition of the electroplating solution utilized is as follows

- $CuSO_4$ - 73 g/l
- H_2SO_4 - 210 g/l
- $CuCl_2$ - 67mg/l
- H2O – Fill up to the 1L mark

The electric current from the current source drives reactions both at the anode and the cathode. At the cathode, copper ions present in the solution are reduced and deposited on the wafer. At the anode, copper in the copper source is oxidized and dissolve into the electroplating solution as copper cations, thereby replenishing the electroplating solution with copper cations. A stirrer is used in the electroplating solution to improve circulation. This enhances plating uniformity and increases plating efficiency.

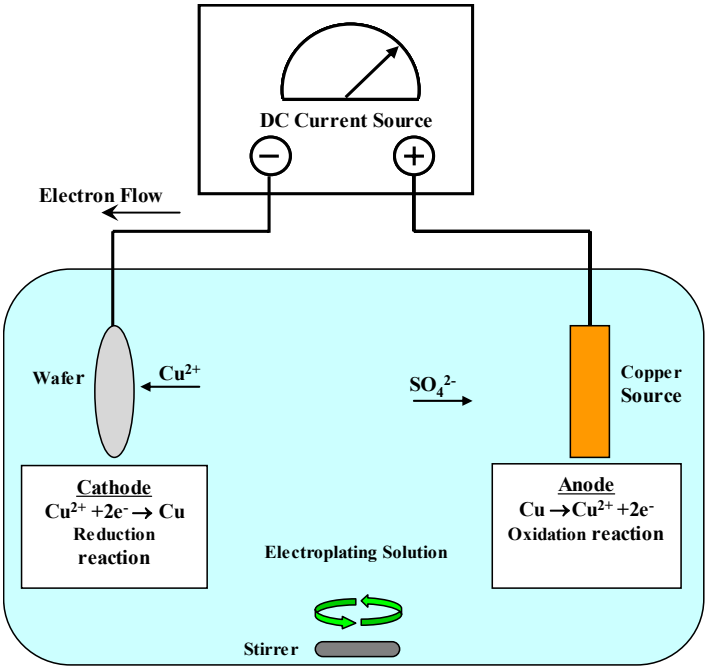


Figure 5.9: Setup for Electroplating Copper [Zhu 2003]

A number of factors are seen to impact the quality of the electroplating process. It is desirable that the electroplating process deposits a homogenous film of uniform thickness. To ensure this, the current density across the wafer must be constant. To achieve this, the cathode and anode are held parallel to each other. The magnitude of the current density also influences the uniformity of plating. A large current density would typically result in a non-uniform plating process. For the current source used in this work, setting it at its minimum current value resulted in an unacceptably high current density. Hence, a copper strip, 50mm in length and 10mm in width, is introduced at the cathode in addition to the wafer. This increased the surface area to be plated at the cathode, hence decreasing the current density to an acceptable value. Also, the surface area of the copper strip is an order of magnitude greater than that of the plating surface on the wafer for both the first layer mask and the second layer mask. Hence, only marginal adjustments needed to made to the current supplied during the first and second electroplating processes as the surface area to be plated is primarily determined by the area of the copper strip which is held constant. For the first electroplating step current is supplied at 15mA for approximately 30 minutes. Towards the end of the electroplating process, the wafer is taken out at regular intervals and the thickness of the electroplated material deposited is measured. This is done to ensure that overplating does not occur. In addition, before every iteration of the electroplating process, the wafer is immersed in a dilute (10%) H_2SO_4 solution for 60 seconds. This removed the thin layer of copper oxide that forms on the surface of the electroplated / sputtered copper. The oxide layer should be removed as it reduces adhesion.

It is observed that for an individual vertical post, the electroplating process is not uniform. Electroplated copper is seen to deposit more rapidly along the edges as compared to the center. This is seen in the fabrication results presented in Figure 5.11.

5.6.3 Seed Layer Deposition

The next step is the deposition of the seed layer of Ti/Cu (30nm/100nm) (Figure 5.1d). The seed layer deposition is done in a Unifilm Sputterer. Deposition is done at a relatively slow rate (peak rate of 7nm/min for Ti and 50nm/min for Cu) to lower the temperature of the wafer during the sputter process. This is important as the seed layer is deposited on a layer of photoresist. It is also advantageous to use the Unifilm because of its short pump down time of approximately 1 minute. This minimizes the oxidation of the top surface of the electroplated copper, improving the adhesion of the seed layer to it. Similar to the electroplating process, before depositing the seed layer, the wafer is dipped in a dilute (10%) H_2SO_4 solution for 60 seconds.

5.6.4 Second Masking Step

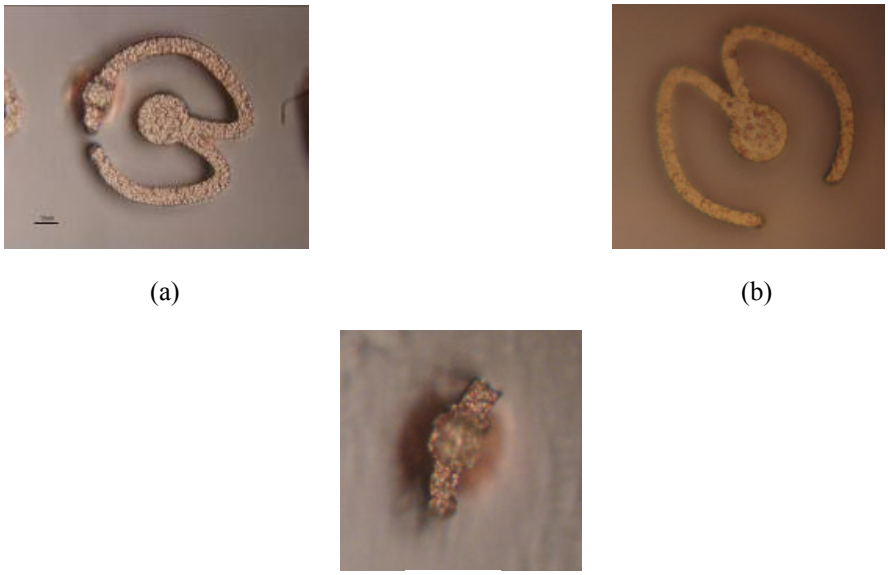
The next step is the deposition and patterning of the second photoresist layer using the second layer mask (Figure 5.1e). NR9-8000P (supplied by Futurrex®) photoresist layer is used for this step. NR9-8000P is used as it is a thicker photoresist compared to NR7-1500P. The data sheet supplied by the manufacturer is used as a guide to determine the process parameters for the photoresist. The photoresist is spin coated on the silicon wafer, the spin speed is 3000rpm with a ramp rate of 1000rpm/sec and a spin time of 40secs, resulting in a photoresist layer that is approximately 8μm thick. The photoresist thickness is not uniform throughout due to the underlying surface. The photoresist is thickest in the center of the post region due to the slight depression introduced by the first plating process. The photoresist is thinnest in the region where the arcuate beam joins the post, due to a slight amount of overplating around the edge of the post. This variation in the thickness of the photoresist has implications for the exposure time and is discussed below. The photoresist dispense step is followed by a pre-bake step in which the wafer is first placed on a hot plate set at 75°C for 5 minutes and then placed on a hot plate set at 110°C for 4 minutes. Subsequently the wafer is placed in a mask

aligner and the photoresist is exposed to UV light through the second layer mask. Again, the mask aligner used is an EV620 mask aligner manufactured by the EV Group (EVG). An exposure time of around 35sec on the EV620 is found to be optimal. The length of the exposure time is critical for this photoresist layer. This is due to photoresist being spun on an underlying seed layer and photoresist layer. A marginal decrease in the exposure time would result in features being overdeveloped and being significantly larger in size than those specified in the mask. This is especially true in the area where the vertical post is present as the photoresist is thickest there. A marginal increase in the exposure time results in photoresist not being removed by the developer in the region where the arcuate beam joins the post. As a result, copper is not electroplated into this region. This introduces a failure mode for the interconnects when they are released (Figure 5.1h), causing them to have discontinuities in that region and is shown in Figure 5.10. Figure 5.10a shows a released interconnect which fails in only one of the arcuate beams. Figure 5.10b and Figure 5.10c show a released interconnect in which failure is observed in both beams. Figure 5.10b shows the post which is still attached to the substrate and Figure 5.10c shows the corresponding arcuate beam section of the interconnect, which is no longer attached to the wafer. After the wafer is exposed on the mask aligner, as part of the post exposure bake, the wafer is placed on a hot plate set at 75°C for 3 minutes. The next step involves the development of the photoresist. RD6 again is utilized as the developer. The wafer is immersed in the developer and the container with the developer is agitated by hand. A develop time of around 25secs is found to be optimal. Like the exposure time, the develop time for NR9-8000P is critical and sensitive to small changes. A long develop time results in exaggerated features, while a short develop time results in photoresist not being removed from the post region of the interconnect (the photoresist is thickest over here). Hence, the wafer is initially placed in the developer for 15 seconds and then placed in the developer in steps of 4 seconds each. Each develop step is interspersed by rinsing the wafer in DI water and then drying the wafer using an air gun.

Completion of the develop step results in the realization of mold patterns for the second layer, comprising of the post, arcuate beams and the circular pad. After the develop process, a "descum" process is run for 1 minute in a Plasma-Therm Reactive Ion Etchant (RIE) to remove any residual photoresist present in the mold openings. The recipe used is the same as that for dry etching NR7-1500P.

Subsequently copper is electroplated into the mold defined by the second photoresist layer. The copper electroplating process is the same as that used for the first photoresist layer. Again, a copper strip is utilized to decrease the current density. A plating current of 15mA is utilized with a plating time of approximately 80 minutes.

After plating copper a thin layer of Ni then Au are plated on top of the copper layer (Figure 5.1g). These layers are necessary for the purpose of assembly. The Ni layer serves as a barrier metal, preventing the formation of intermetallic compounds between the solder and the copper. These intermetallic compounds are not desirable as they are detrimental to interconnect reliability. The Au layer prevents oxidation of the underlying Ni/Cu layers and provides a wettable surface for the purpose of assembly. Electroplating of these layers is also done using the copper strip. Ni is plated at 15mA for 10 minutes and Au is plated at 3mA for 3 minutes.



(a) (b)

(c)

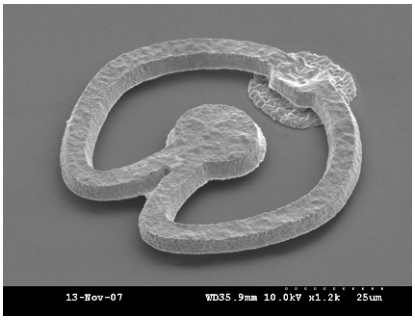
Figure 5.10: Failure in Arcuate Beam Due to Overexpsure of Second layer Photoresist

5.6.5 Release of Interconnect

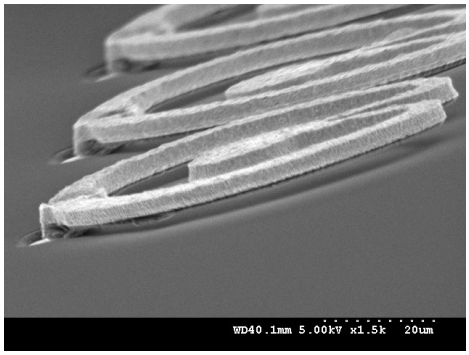
After the interconnect has been fabricated the next step is to release it. First, the second photoresist layer of NR9-8000p is removed by immersion in acetone. This is followed by removing the Ti/Cu seed layer. The Cu seed layer is removed by using Aluminum Etchant Type A (supplied by Transene Inc.). The Ti seed layer is removed by using BOE. Removal of the first photoresist layer, NR7-1500p is more challenging. Due to the subsequent processing steps performed after it is patterned, the photoresist cannot be removed by immersion in acetone. RR4 resist remover, recommended and supplied by Futurrex, is tried but is also unable to remove the photoresist. Finally, an acetone bath placed in a sonicator is found to remove the photoresist. The process of removal of the first layer photoresist takes about 1 minute. Once this photoresist layer is removed, free-standing FlexConnects are realized.

5.7 Fabrication Results

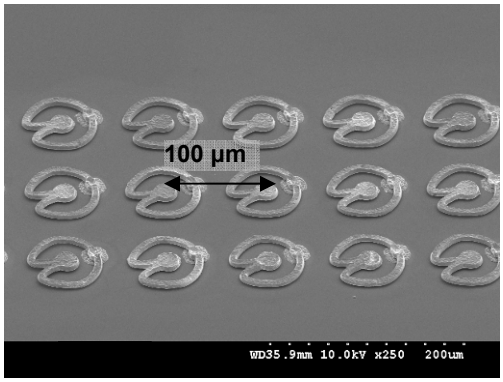
Micrographs are taken of FlexConnects fabricated at a 100 µm pitch in a three row peripheral array format for a die size of 20 mm X 20 mm. Fabrication results are shown in Figure 5.11. The fabrication is observed to be uniform across the wafer as well as repeatable.



Top View



Side View



Zoomed Out View

Figure 5.11: Parallel-Path FlexConnects Fabricated at a 100µm Pitch

5.8 Conclusions

In this chapter, a MEMS-based fabrication process is developed to realize the interconnect design described in Chapter 4. Sequential lithography and electroplating processes with up to two masking steps are utilized as part of the fabrication process. Such an approach potentially reduces the cost of fabricating compliant interconnects. The approach is implemented to fabricate parallel-path FlexConnects at a 100 μm pitch in a three-row peripheral array format with for a 20 mm x 20 mm die size. The fabrication process parameters are optimized and resulted in a fabrication process which had excellent yield across a 4 inch wafer with interconnects that are uniform and repeatable. Although in this work only a peripheral array of interconnects are realized, the fabrication process can easily be implemented to realize FlexConnects at a 100 μm pitch in a full area-array format.

CHAPTER 6
VARIABLE INTERCONNECT GEOMETRIES

6.1 Introduction

As describe in Chapter 4, one of the challenges associated with compliant interconnects is its inferior electrical performance compared to an equivalent solder bump. One approach to address this limitation is to innovate on the design of an individual compliant interconnect. Such an approach has been developed and discussed in Chapter 4. Alternatively, adopting a system level view towards designing compliant interconnects provides another avenue to address the limitations in their electrical performance. To enable this system level view, advantage is taken of the photolithographic techniques used to fabricate a number of compliant interconnects, including G-Helix interconnects and FlexConnects. As photolithographic techniques are used to define their geometry, compliant interconnects provide excellent opportunities for cost-effective I/O customization based on electrical and mechanical requirements. Consequently, this presents a unique opportunity to tailor the system performance by balancing electrical requirements against mechanical reliability concerns by varying the interconnect geometry across a single die.

In this chapter, a concept based on varying the interconnect geometry across a single die is developed (Section 6.2). G-Helix interconnects are considered as a test case. The fabrication process to realize this concept is discussed (Section 6.3 and Section 6.4). To illustrate the advantages of employing varied interconnect geometries, the mechanical and electrical characteristics of three different interconnect geometries are then determined (Section 6.5) and the thermo-mechanical reliability of an electronic package employing such a varied interconnect geometry is evaluated (Section 6.6). Subsequently, the influence of the interconnect geometry on stresses introduced in the die are calculated (Section 6.7). Finally, the variable interconnect geometry concept is extended to FlexConnects (Section 6.8).

6.2 Integrative Solution

In general, changing the geometric parameters of a compliant interconnect have opposing effects on desirable electrical and mechanical performance parameters. In other words, when a geometric parameter is changed to improve the mechanical compliance, the self-inductance and the resistance increase. For example, when the G-Helix interconnects thickness or width is decreased, the mechanical compliance increases; however, the self-inductance and the electrical resistance also increase [Zhu et al. 2004]. Thus, by using different dimensions and different geometries for the interconnects, their mechanical and electrical performance can be optimized, and therefore, the power and latency challenges described in Chapter 1 can be addressed without compromising on the mechanical reliability of the interconnects. Also, as the interconnects are defined through a lithographic process, different interconnect geometries can be fabricated without an increase in the number of processing steps.

In general, the interconnects near the center of the die need not have a high mechanical compliance as the differential displacement between the die and the substrate due to CTE mismatch is low near the center of the die. Thus, the interconnects at the center of the die can be fabricated in the shape of a column structure, while the interconnects near the edge of the die can be fabricated with compliant interconnect structure. The column structures have lower electrical parasitics associated with them as compared to the compliant interconnects. In addition, the central columns can be beneficial from a number of perspectives: (1) They can be used predominantly as ground-power interconnects with the ability to carry higher current densities, (2) They can provide high enough rigidity against potential vibration or drop induced damage on the compliant interconnects, (3) They can act as a stopper to prevent damage to the compliant interconnects when an excessive force is inadvertently applied either during assembly and/or when a heat sink is attached. As these columns are located near the center of the die where the CTE-induced differential thermal expansion is low, these columns will

neither fatigue fail nor exert excessive force on the low-K dielectric to crack or to delaminate. The interconnects away from the center of the die can be fabricated with increasing magnitude of compliance as one traverses to the corner/edge of the die. Typically, near the corner of the die, the CTE-induced differential thermal deformation is high, and therefore, higher compliance is needed to reduce the force induced on the die pads by the interconnect. These compliant interconnects towards the edge of the die can be used as signal interconnects. Between the column interconnects near the center and highly-compliant interconnects near the edges of the die, the interconnects in the middle region can be designed with intermediate compliance.

To demonstrate the advantages and viability of such an approach G-Helix interconnects will be considered as a test case. A description on G-Helix interconnects is provided in Section 2.4.5. A schematic illustration of G-Helix interconnects is provided in Figure 6.1.

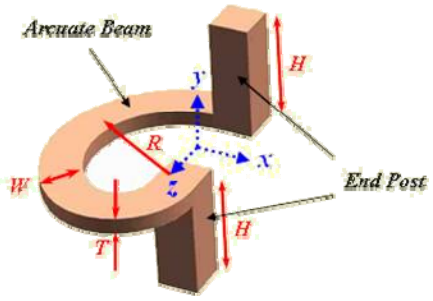


Figure 6.1: Schematic of a G-Helix Interconnect

The proposed integrative solution with varying compliance is different from the mixed-bump concept pursued and patented elsewhere [King and Wilcox 1975; Lin and Winter 1975; Potter et al. 2002; Caletka and Johnson 2003]. Under the mixed-bump concept, rotationally-symmetric solder bumps with different diameters are used between the die and the substrate. Such mixed bumps will require underfill, especially for larger dies and when organic substrates are used. Furthermore, such bumps typically have a compliance of the order 0.01 mm/N, which is several orders of magnitude smaller than

the compliance of the proposed interconnects. Such solder bumps when used with underfill will create high stresses in the die and will lead to cracking and/or delamination of low-K dielectric material in future dies. Also, utilizing an underfill material limits the compliance of the interconnect. In addition, the presence of an underfill, for the purposes of thermo-mechanical reliability, adds process costs and time. On the other hand, compliant interconnects do not require an underfill for thermo-mechanical reliability. They can be scaled to finer pitches, as they use lithographic processes. They can be tailored to have different compliance from center to the edge of the die such that the thermo-mechanical and electrical performance is optimized. Using masking process, the proposed concept opens up the possibility of compliant interconnects with different shapes, orientations, and dimensions.

6.3 Simultaneous Fabrication of Varying Interconnect Geometries

The fabrication process for G-Helix interconnects is described in Figure A.1 Sequential lithography and electroplating plating steps are used to fabricate G-Helix interconnects. The fabrication process uses three masking steps. To realize variable interconnect geometries the G-Helix fabrication process is modified as shown in Figure 6.2.

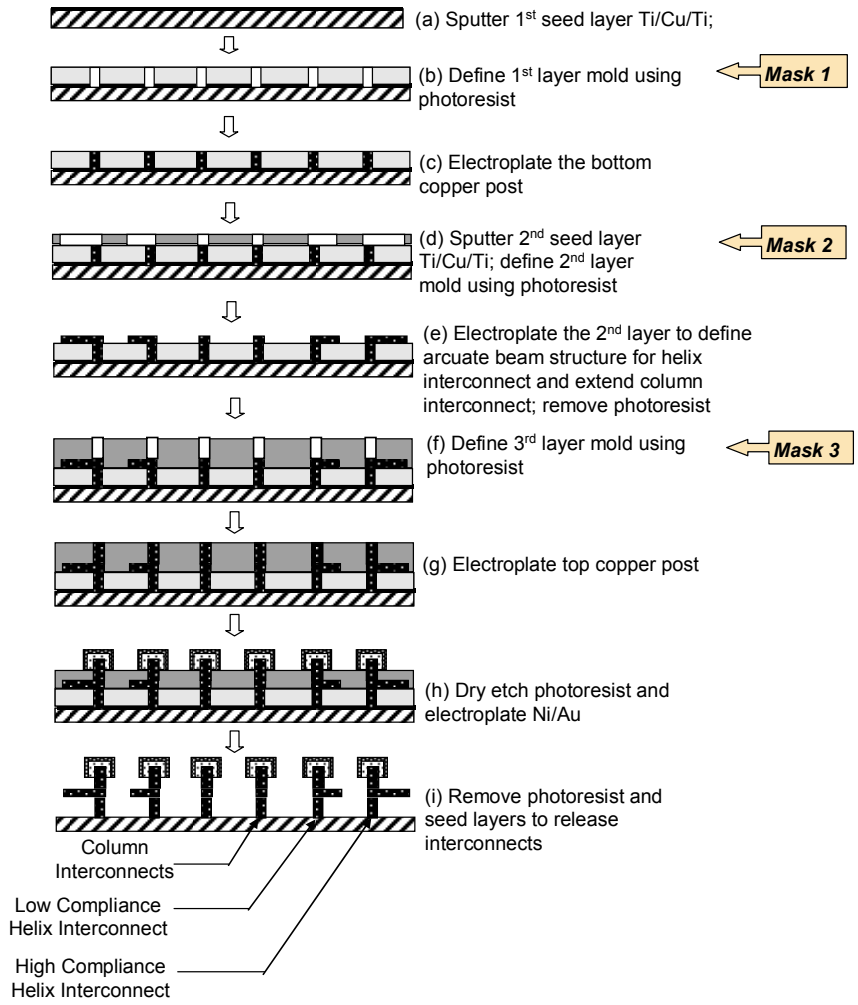


Figure 6.2: Fabrication Process for Variable Interconnect Design

A brief description of the fabrication process is provided below. To begin the fabrication of the heterogeneous interconnects, on a given clean Si wafer, a Ti/Cu/Ti (30nm / 100nm / 30nm) seed layer is sputter deposited. The bottom and the top Ti layers are present to improve the adhesion between wafer/Cu and Cu/applied photoresist interfaces. After the Ti/Cu/Ti seed layer deposition, a layer of SU8 photoresist is spun, exposed, and developed to define the first layer mold for the bottom post. The thickness of the SU8 layer is approximately 35μm. After etching away the top Ti layer of the seed layer, copper is electroplated to realize the bottom post. After electroplating, a second Ti/Cu/Ti (30nm/100nm/30nm) seed layer is sputter-deposited and a layer of NR9-8000P photoresist is spun. The thickness of the NR9-8000P photoresist is approximately 8μm.

The second layer of photoresist is used to define the different geometries for different interconnects: interconnects near the center of the die will have column geometries aligned with the bottom post, the interconnects near the edges of the die will have the G-Helix geometry to provide high compliance, and the interconnects in the middle will have the G-Helix geometry with increased width to provide intermediate compliance and decreased electrical parasitics. Once the photoresist is developed and the seed Ti layer is etched, copper can be electroplated into the molds and the varied geometries can be simultaneously realized. The sequential process of photolithography and electroplating is repeated once more to create the top post for the interconnects. Once the steps are completed, the surrounding photoresist and seed layers can be etched to create the free-standing compliant interconnects. In summary, a three-mask process is used to create interconnects that vary in shape from the center to the edge of a die: from column to low-compliant helix interconnects to high-compliant helix interconnects, and still maintaining the 100μm pitch through the entire array.

6.4 Fabrication Results

Using the fabrication process described above, such variable interconnect geometries are fabricated. The interconnects are fabricated on a 4 inch silicon wafer. A schematic representation of the mask used is shown for an individual die in Figure 6.3. Pink denotes the first layer mask, yellow denotes the second layer mask, and blue denotes the third layer mask. The die size is 10 mm x 10 mm, with interconnects present in an area array configuration at a 100μm pitch. Column interconnects are present at the center of the die. High-compliant G-Helix interconnects are present near the edges of the die. The intermediate region between these two interconnect designs is occupied by low-compliant G-Helix interconnects.

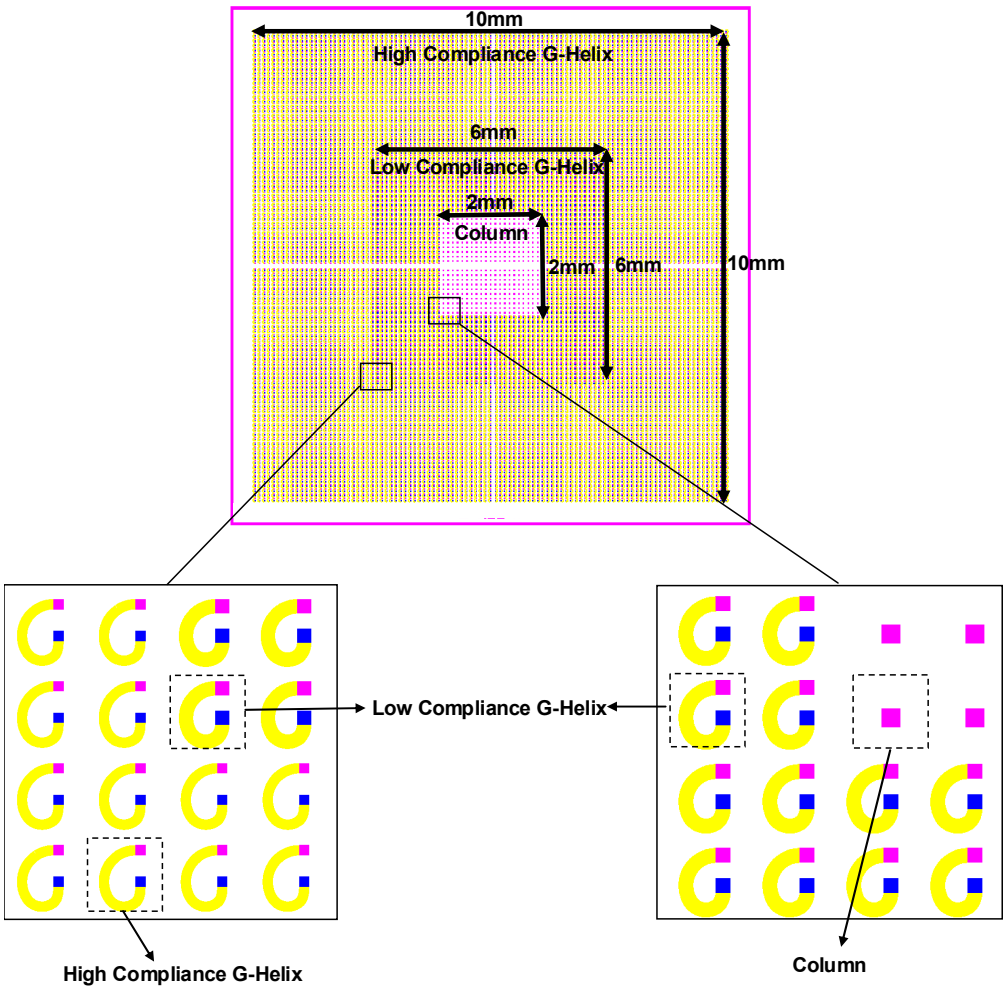


Figure 6.3: Schematic Representation of Variable Compliance Mask Design for Interconnects at a 100µm pitch

The fabricated structures are shown in Figure 6.4 and Figure 6.5. As seen in Figure 6.4, column interconnects are present at the center of the die, high compliant interconnects are present towards the edge and low-compliant interconnects are present in the intermediate region. Figure 6.5 shows additional images of these fabricated structures. Figure 6.5a shows adjacent column and low-compliant helix interconnects. Figure 6.5b shows adjacent high-compliant G-Helix and low-compliant G-Helix interconnects.

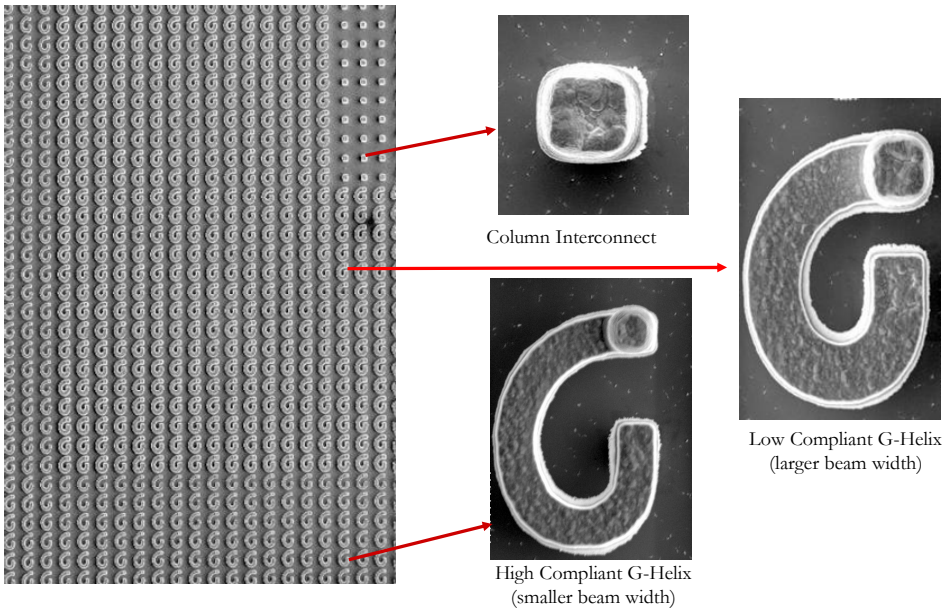


Figure 6.4: Varying Interconnect Geometries Fabricated at a 100µm Pitch

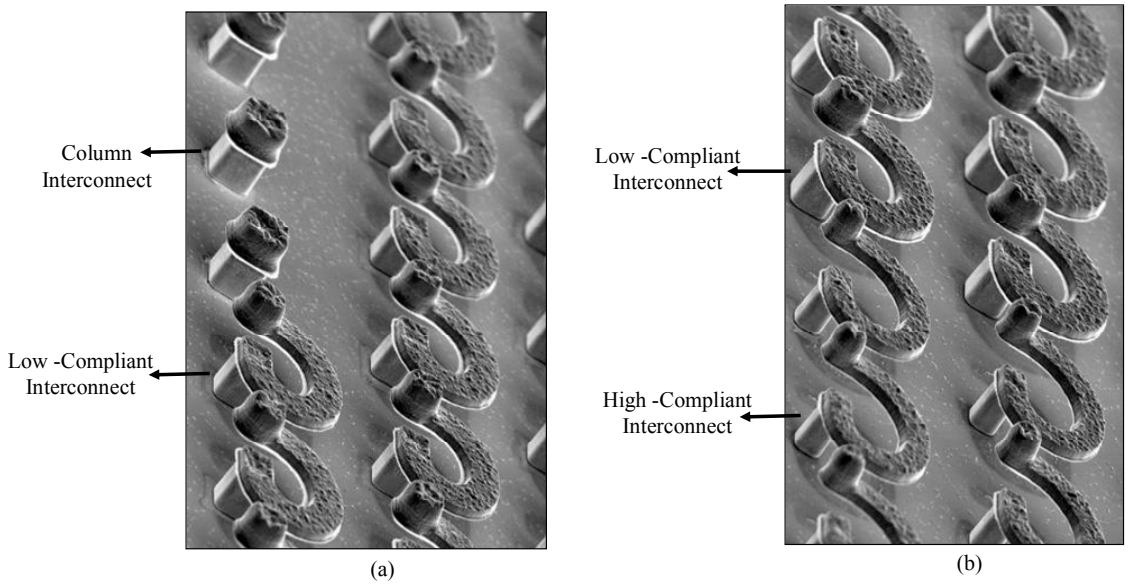


Figure 6.5: Magnified View of Varying Interconnect Geometries Fabricated at a 100µm Pitch

6.5 Electrical and Mechanical Performance of Interconnects

To demonstrate the advantages of varying the interconnect geometries, numerical models are developed in a finite element package (ANSYS) to represent three different packages. In the first package (*Package 1*), column interconnects with a square cross-

section (20 μm x 20 μm) are populated throughout the die in a similar 100 x 100 area-array configuration. In the second package (*Package 2*), identical high-compliant G-Helix interconnects are populated throughout the die in a 100 x 100 area-array configuration. The high-compliant interconnects have a stand-off height of about 78 μm, beam width (W) of 11 μm and arcuate radius of 36 μm. In the third package (*Package 3*), the center of the die is populated with column interconnects, the peripheral rows are populated with high-compliant G-Helix interconnects, and the area in-between is populated with low-compliant G-Helix interconnects. The low-compliant interconnects have a beam width (W) of 15 μm and arcuate radius of 36 μm. The interconnects form a 100 x 100 area array, and as one traverses from the center of the die to one of the edges of the die, there are 10 rows of column interconnects, 15 rows of low-compliant interconnects, and 25 rows of high-compliant interconnects. This corresponds to the interconnect configuration discussed in the previous section for which fabrication results were presented.

The mechanical and electrical characteristics of the three different interconnect geometries (column, low-compliant G-Helix, high-compliant G-Helix) are determined. The mechanical performance of the interconnects is characterized in terms of their out-of-plane compliance c_y and in-plane diagonal compliance $c_d = ((c_x^2+c_z^2)/2)^{0.5}$. x and z are the in-plane directions as shown in Figure 6.1. To determine the compliance of the G-Helix interconnects, closed form solutions developed in [Zhu et al. 2004] are used. Compliance values are also obtained using finite element based simulations. Material properties for copper, described in Section 4.6 are used. Depending on the choice of method and boundary conditions, the diagonal compliance of the high-compliant interconnects are seen to vary between 7mm/N and 9mm/N, and the out-of-plane compliance varies between 7 mm/N and 11.5 mm/N. Similarly, the diagonal compliance of the low-compliant interconnects are seen to vary between 3.5mm/N and 4.5mm/N, and the out-of-plane compliance varies between 5.5 mm/N and 6.5 mm/N. For determining the diagonal compliance of the column interconnects, they are considered as a beam with a force

applied at its end. For determining the out-of-plane compliance the column interconnects is considered as a rod with an axial load applied at its end. The electrical performance is qualitatively described in terms of the resistance and the inductance of the interconnects. The resistance and self-inductance of the interconnects are determined through numerical simulations in FastHenry. The resistivity of copper is taken as 1.772×10^{-6} Ω-cm. The obtained mechanical and electrical characteristics of the three interconnect geometries are summarized in Table 6.1.

Table 6.1: Mechanical and Electrical Characteristics of Interconnect Geometries

	Electrical Characteristics		**Mechanical Characteristics**	
	R_{DC} **(mΩ)**	L_{self} **(pH)**	C_d **(mm/N)**	C_y **(mm/N)**
Column Interconnects	3.47	30.95	0.10	0.0016
Low-Compliant Helix Interconnect	30.15	84.44	3.5 to 4.5	5.5 to 6.5
High-Compliant Helix Interconnect	42.65	92.73	7 to 9	7 to 11.5

As seen, the column interconnects have lower electrical parasitics, and thus, superior electrical characteristics, while the high-compliant interconnects have higher mechanical compliance, and thus, superior mechanical characteristics. The low-compliant interconnects have better mechanical characteristics than the column interconnects, though their electrical characteristics are inferior. When compared with the high-compliant helix interconnects, the low-compliant helix interconnects have better electrical characteristics and inferior mechanical characteristics.

6.6 Thermomechanical Reliability Modeling

A popular approach to evaluate the thermo-mechanical reliability of interconnects is to develop finite element models representing the interconnects as part of an electronic

package. Three types of geometry models are commonly adopted to model electronic packages: 1) 2D Models 2) 2.5D Models 3) 3D Models. The choice of the model is based on the accuracy desired, the results desired from the model and the limitations imposed by computing resources. 2D models, computationally the "cheapest", represent a cross-section of the package. However, as the G-Helix interconnect is a 3D structure whose geometry cannot be adequately captured by a single cross-section. Hence 2D models are typically not used. 2.5D Model, also referred to as Generalize Plane Displacement (GPD) models, represent a compromise between 2D and 3D models. These models are computationally more intensive than 2D models, but are able to capture the 3D interconnect geometry and are hence more accurate. Compared to 3D models, they are computationally less intensive. In a 2.5D model, a predetermined width is modeled with 3D elements representing a strip of the package. The width of the strip is typically equal to the pitch of the interconnects. The remaining package geometry is approximated by applying appropriate boundary conditions. In a 3D model, no geometric assumptions are made, and the complete geometry of the package is represented. A quarter or $1/8^{th}$ symmetry model with appropriate symmetry boundary conditions can be used. However, 3D models are not always a feasible approach due to the computational demands imposed by it.

Material models are also needed to capture the behavior of materials comprising the modeled package. The choice of material model is governed by the behavior of the material under the given loading conditions. For example, under typical accelerated thermal cycling (ATC) tests, silicon would be modeled as a linear elastic material, copper modeled using an elastic-plastic constitutive model and solder modeled using an appropriate constitutive model (creep model with plasticity or a viscoplasticity model such as Anand's model) that captures the creep behavior of solder.

Once the geometry and the material models are created and the boundary conditions are applied, the thermal loading conditions are then applied on the model to

determine the thermally-induced stress-strain distribution in the geometry. The process temperature profile (assembly and cool down) is initially applied. Typically the solder reflow temperature is taken as the stress-free temperature. Subsequently, the ATC profile is applied. All the ATC cycles are normally not simulated. This is because the stress-strain profile stabilizes after a few thermal cycles with regards to the damage parameter and hence the subsequent cycles do not need to be modeled. The results from the last modeled thermal cycle are used to calculate the appropriate damage parameter.

Under field-use conditions or under thermal cycling, the compliant interconnects experience repeated thermo-mechanical loads due to the CTE mismatch between the substrate and die and will fatigue fail. Also, the fatigue failure of compliant interconnects is typically in the low-cycle fatigue regime and determines the life prediction model used. In general, variations of a Coffin-Manson equation are utilized to predict the low cycle fatigue life of metals. The damage metric utilized is either strain based or energy based. The general form of the Coffin-Manson equation [Suresh 1998] follows

$$N_f = A(\Delta\varepsilon_{in})^m \qquad \textbf{(6.1)}$$

where N_f is the number of cycles to failure, $\Delta\varepsilon_{in}$ is the inelastic strain range and m, A are constants. In this form of the Coffin-Manson equation, the inelastic strain range is utilized as the damage metric. Other damage metrics utilized include accumulated inelastic strain, accumulated creep strain, strain energy density, creep strain energy, and other variations. When an energy based criterion is utilized in the form given by Equation 6.2, it is known as a Morrow equation [Suresh 1998].

$$N_f = B(\Delta W)^n \qquad \textbf{(6.2)}$$

where N_f is the number of cycles to failure, ΔW is the energy based criterion and n, B are constants. The relationship drawn between the number of cycles to failure and the damage metric is generally obtained through a regression analysis of experimentally

obtained failure data. Using the model developed the damage parameter is evaluated and the fatigue life of the interconnects predicted.

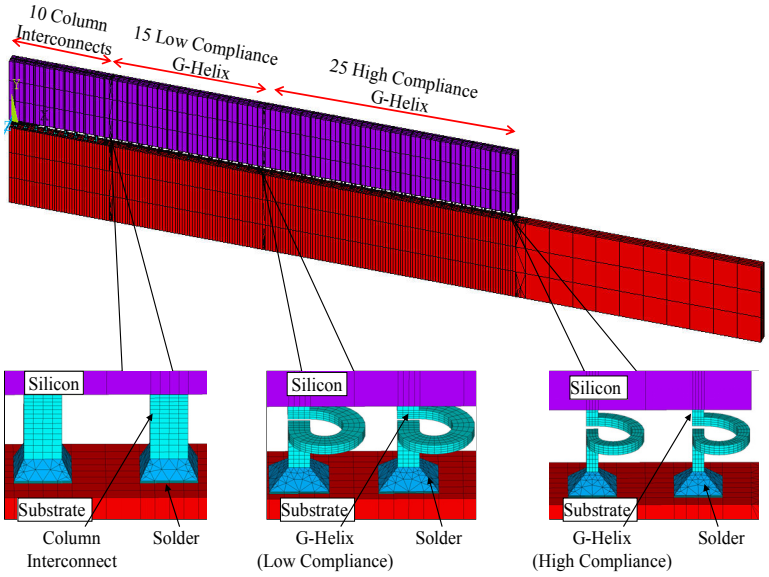


Figure 6.6: Meshed GPD Model of Variable Interconnect Geometries (*Package 3*)

To assess the thermomechanical reliability of the three packages, Generalized Plane Displacement (GPD) models are developed for each of them taking into consideration the silicon die, the interconnects, the solder attach, and the organic substrate. An example GPD model of *Package 3*, comprising of a heterogeneous combination of interconnects is shown in Figure 6.6. GPD models have been successfully used in literature [Gustafsson et al. 2000; Classe and Sitaraman 2003; Yeo et al. 2006] and are particularly useful to compare trends among different geometries, different designs, etc.

In the GPD model, the copper helix interconnect was modeled as a temperature-dependent multi-linear kinematic hardening material. [Iannuzzelli 1991] provides elastic-plastic properties which represent electroplated copper with thickness greater than 15 μm. As the helix interconnects are fabricated by electroplating copper and have a thickness of the same order of magnitude, it is reasonable to use the data from [Iannuzzelli 1991]. The

silicon die (600μm thick) is modeled as isotropic, linear elastic and temperature dependent. The organic substrate (800 μm thick) is modeled as orthotropic, linear elastic and temperature dependent. In this model, the solder is assumed to be Sn96.5Ag3.5, and is modeled as viscoplastic [Wang et al. 2001]. Detailed material property data is described in Appendix B. The mesh density used for all three interconnect geometries was the same to be able to compare the strain results among the different interconnects.

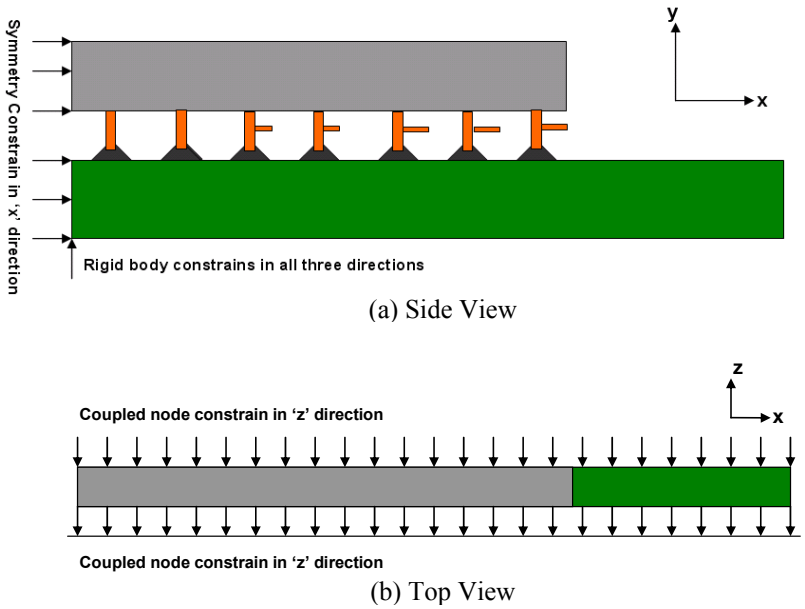


Figure 6.7: Boundary Conditions on GPD Models

Symmetry conditions are applied along the *x*–symmetry plane and *z*-face nodes are coupled in deformation along *z* axis. Also, the left bottom corner of the assembly is fully constrained to prevent rigid body motion. These boundary conditions are illustrated in Figure 6.7.

The thermal loading is simulated as follows: The package is first subjected to a load step from solder melting temperature to room temperature; it is then dwelled for an hour at room temperature. The SnAg solder melting temperature (220°C) is taken as the stress-free temperature. Next, the package is subjected to accelerated thermal cycles between 0°C and 100°C with five minute dwells. The stress-strain behavior stabilized

after three cycles, and therefore, the results from the third cycle are used for further analysis.

The plastic strain distribution for all three packages at the end of the third thermal cycle is provided in Figure 6.8. As can be seen, in both *Package 1* and *Package 2*, the maximum plastic strain is observed in the outermost interconnect. This is also true of *Package 3*, in which the maximum plastic strain is observed in the outermost high-compliant G-Helix interconnect rather than the outermost low-compliant G-Helix interconnect or the outermost column interconnect.

Coffin-Manson-type equation, derived using experimental data for electroplated copper [Engelmaier 1982], is used to determine the fatigue life of the compliant interconnects and is given as:

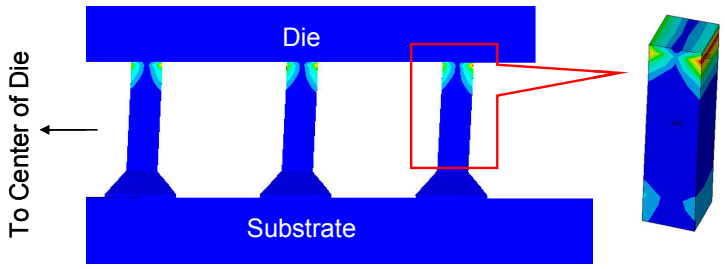
$$N_f^{-0.6} \times \varepsilon_f^{0.75} = \Delta\varepsilon_p \qquad \textbf{(6.3)}$$

N_f: Mean cycles to failure

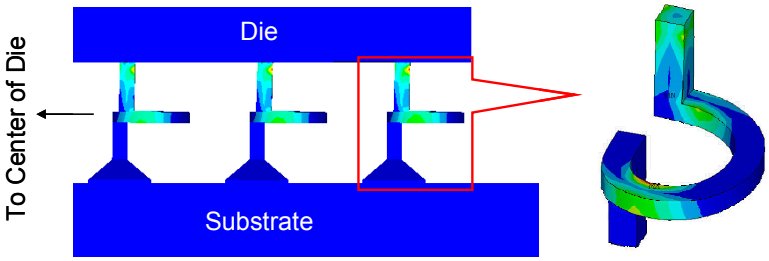
$\Delta\varepsilon_p$: Plastic strain range

ε_f: Fatigue ductility coefficient

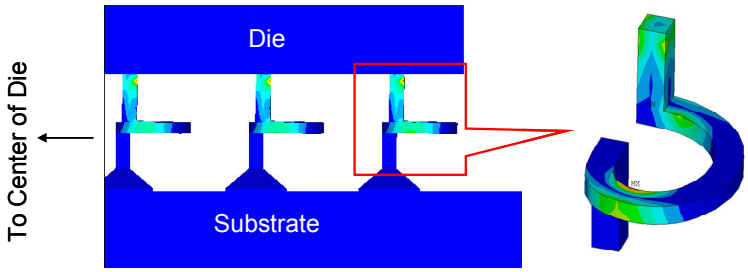
The fatigue ductility coefficient for copper was reported to vary from 0.15 to 0.3 [Prabhu et al. 1995].



(a) Package 1 – Column Interconnects



(b) Package 2 – High-Compliant G-Helix Interconnects



(c) Package 3 – Heterogeneous Interconnects

Figure 6.8: Equivalent Plastic Strain Distribution at the End of 3rd Thermal cycle

From the plastic strain component in various parts of the assembly, the fatigue life of the compliant interconnect as well as the solder joint is determined, and it was found that the fatigue failure was likely to occur in the copper interconnects, rather than the solder joints, as intended in the design. In other words, the compliant interconnects are designed to accommodate the differential displacement induced through the CTE mismatch between the die and the substrate and are designed to alleviate the high plastic deformation in the solder joints.

Based on Equation 6.3, the estimated fatigue life of the three different packages along with the strain range and location of failure is provided in Table 6.2. As can be seen from Table 6.2, $N_{50\%}$ (mean life to fatigue failure) values of the interconnects in *Package 2* and *Package 3* are approximately equal. However $N_{50\%}$ of *Package 1* is much lower. This is because the column interconnects are not compliant, and are not able to accommodate the CTE mismatch at the outermost locations. Although *Package 2* is good from a thermomechanical reliability perspective, it is not recommended from an electrical performance viewpoint due to the higher electrical parasitics associated with the high-compliant interconnects. Therefore, *Package 3* represents a judicious trade-off between electrical parasitics and mechanical reliability.

Table 6.2: Estimated Fatigue Life and Fatigue Failure Location

Package 1 *Column Interconnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	0.6670
	Predicted $N_{50\%}$	748
	Location of failure	Die Side
Package 2 *High-Compliant Helix Interconnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	0.3057
	Predicted $N_{50\%}$	2745
	Location of failure	Arcuate Beam
Package 3 *Heterogeneous Interconnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	0.2833
	Predicted $N_{50\%}$	3118
	Location of failure	Arcuate Beam

6.7 Compatibility with Low-k Dielectric's

Numerical simulations were also performed to examine if the developed interconnects will be beneficial for ICs with low-K dielectric material. To demonstrate this, the generalized plane-deformation (GPD) finite-element models for *Packages 1, 2, and 3,* described in the previous section, were utilized. The boundary conditions and material properties are kept the same as before.

Figure 6.9: σ_{xx} Stress in the Die

Table 6.3: Die Stresses at -55°C after Reflow

		σ_{xx} (MPa)	σ_{xy} (MPa)	σ_{yy} (MPa)
Package 1 *Column Interconnects*	*Max*	15.920	2.298	5.41
	Min	-18.11	-1.767	-1.021
Package 2 *High-Compliant Helix Interconnects*	*Max*	1.771	0.519	1.575
	Min	-2.440	-0.888	-1.645
Package 3 *Heterogeneous Interconnects*	*Max*	4.126	0.716	3.818
	Min	-7.254	-1.472	-2.818

The solder melting temperature (220°C) is taken as the stress-free temperature as before, and all the three packages are simulated to be cooled down from the stress-free temperature to -55°C. Figure 6.9 shows the stress contours in the die at -55°C for the

three configurations. The results are summarized in Table 6.3. Table 6.3 shows the stresses induced in the die, and it is seen that the stresses induced in *Package 2* and *Package 3* are an order of magnitude of lower than the stresses in flip-chip dies with underfill. Also, the die stresses in *Package 2* and *Package 3* are lower than the die stresses in *Package 1*. These trends are along expected lines. *Package 1* has the stiffer column interconnects and hence exhibits the highest die stresses. For both the packages with compliant helix interconnects (*Package 2* and *Package* 3), it was observed that the magnitude of the stresses introduced in the die was less than 5 MPa. Thus, the low-K dielectric material is not likely to crack or delaminate, as the G-Helix interconnects create significantly lower stresses in the die by decoupling the die from the substrate.

On the other hand, for flip-chip on organic board assemblies with underfills, simulations with identical die/substrate dimensions indicate that the die stresses will be of the order of 140 MPa (Figure 6.10). The stand-off height for the solder bumps was 60µm. The underfill was modeled as a linear elastic material with an elastic modulus of 7.8GPa, Poisson's ratio of 0.33 and CTE of 28ppm.

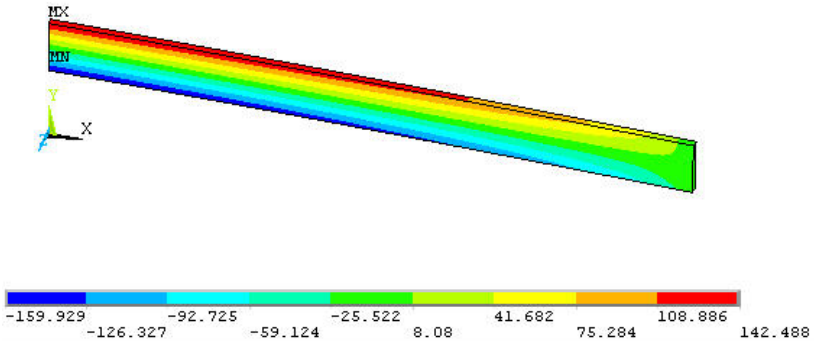


Figure 6.10: σ_{xx} Stresses in the Die at -55°C for Flip-Chip with Underfill

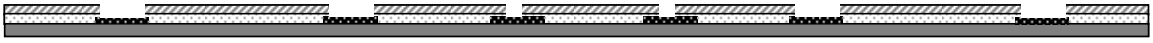
6.8 Varying Interconnect Geometries and FlexConnects

In previous sections of this chapter it has been shown that employing interconnects with varying geometries across a single die is beneficial. G-Helix interconnects were considered as an example. Two principal reasons allow this approach

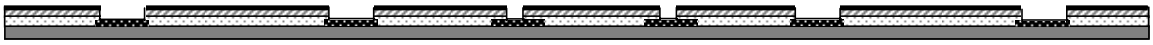
to be useful and viable – the lack of an underfill material and the use of photolithographic techniques to fabricate the interconnect. FlexConnects, described in Chapter 4 and Chapter 5, also share both these characteristics. Hence, the varying compliance approach can be adapted to them as well. To enable this, the fabrication process for FlexConnects described in Figure 5.1 can be modified as illustrated in Figure 6.11 .

(a) Start with an IC wafer having die pads.

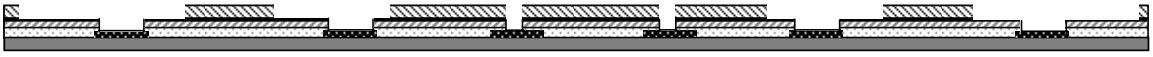
(b) Deposit blanket film of passivation material.



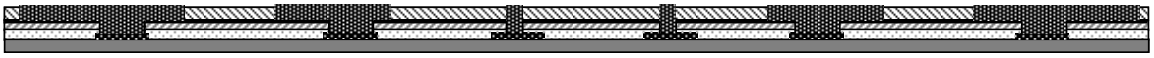
(c) Spin coat and pattern first photoresist layer. Etch openings in passivation layer.



(d) Sputter deposit seed layer.



(e) Spin coat and pattern second photoresist layer to define molds for arcuate structure of FlexConnects and extending column interconnects.



(f) Electroplate metal into molds defined by both photoresist layers.

(g) Electroplate Interface metal layer.

(h) Strip photoresists and etch seed layer to release interconnects.

Figure 6.11: Fabrication of Variable Interconnect Design with FlexConnects

To illustrate the benefits of implementing this approach for the case of FlexConnects, the electrical and mechanical characteristics of three geometries are

considered – parallel-path FlexConnects as shown in Figure 4.4 (beam width = 4 μm) alternatively referred to as high-compliance FlexConnects, parallel-path FlexConnects with a wider beam (beam width = 6 μm) alternatively referred to as low-compliance FlexConnect, and column interconnect (height = 10 μm, 4 μm x 4 μm square cross-section). The height of the column interconnect is restricted to 10μm by the fabrication process employed for FlexConnect. Similar to the case of G-Helix interconnects, column interconnects would be employed in the center of the die, high-compliance FlexConnects towards the edge of the die, and low-compliance FlexConnects would be employed in the intermediate region. Mechanical compliance values for FlexConnects are obtained using finite element based simulations. For determining the compliance of the column interconnects, they are considered as a beam with a force applied at its end. The resistance and self-inductance of the interconnects were determined through numerical simulations in FastHenry. The obtained mechanical and electrical characteristics of the three interconnect geometries are summarized in Table 6.4.

Table 6.4: Mechanical and Electrical Characteristics of Interconnect Geometries for FlexConnects

	Electrical Characteristics		**Mechanical Characteristics**		
	R_{DC} **(mΩ)**	L_{self} **(pH)**	C_x **(mm/N)**	C_z **(mm/N)**	C_d **(mm/N)**
Column Interconnects	11.11	3.21	1.3	1.3	1.3
Low-Compliance FlexConnect	29.0	34.6	0.70	2.10	1.57
High-Compliance FlexConnect	40.94	36.5	2.15	6.47	4.82

As expected, the column interconnects have lower electrical parasitics, and thus, superior electrical characteristics, while the high compliance FlexConnects have higher mechanical compliance, and thus, superior mechanical characteristics. The low compliance FlexConnects have better mechanical characteristics than the column interconnects, though their electrical characteristics are inferior. When compared with the high compliance FlexConnects, the low compliance FlexConnects have better electrical characteristics and inferior mechanical characteristics. For the simulations conducted, solder used to assemble the interconnects is neglected. Taking it into consideration would not influence the characteristics of the FlexConnects significantly. However, due to the relatively smaller dimensions of the column interconnect, considering solder would have a significant effect, increasing the electrical parasitics of the interconnect and decreasing the mechanical compliance.

To demonstrate the advantages of varying the interconnect geometries for the case of FlexConnects, numerical models are developed in a finite element package (ANSYS) to represent three different packages. In the first package (*Package 1*), column interconnects (with dimensions as described before) are populated throughout the die in a similar 100 x 100 area-array configuration. In the second package (*Package 2*), identical high-compliance FlexConnects are populated throughout the die in a 100 x 100 area-array configuration. In the third package (*Package 3*), the center of the die is populated with column interconnects, the peripheral rows are populated with high-compliance FlexConnects, and the area in-between is populated with low-compliance FlexConnects. The interconnects form a 100 x 100 area array, and as one traverses from the center of the die to one of the edges of the die, there are 5 rows of column interconnects, 20 rows of low-compliance interconnects, and 25 rows of high-compliance interconnects. To assess the thermomechanical reliability of the three packages a procedure similar to that used for G-Helix interconnects is utilized. Generalized Plane Displacement (GPD) models are developed for each of them taking into consideration the silicon die, the interconnects,

the solder attach, and the organic substrate. The material models, boundary conditions and loading conditions are identical to that used for G-Helix interconnects. For both *Package 1* and *Package 2*, the maximum plastic strain is observed in the outermost interconnect. This is also true of *Package 3*, in which the maximum plastic strain is observed in the outermost high-compliance FlexConnect rather than the outermost low-compliance FlexConnect or the outermost column interconnect. From the plastic strain component in various parts of the assembly, the fatigue life of the compliant interconnect as well as the solder joint is determined, and it was found that the fatigue failure was likely to occur in the copper interconnects, rather than the solder joints, as intended in the design.

Based on Equation 6.3, the predicted fatigue life of the three different packages along with the strain range and location of failure is provided in Table 6.5. As can be seen from Table 6.5, $N_{50\%}$ (mean life to fatigue failure) values of the interconnects in *Package 2* and *Package 3* are approximately equal. However $N_{50\%}$ of *Package 1* is significantly lower, even when compared to the case of *Package 1* for G-Helix interconnnects. This is because the column interconnects have a low stand-off height and are not compliant, and hence are not able to accommodate the CTE mismatch at the outermost locations. For the same reason, *Package 3* has 5 rows of column interconnects, as otherwise the column interconnect would fail before the high-compliance FlexConnect. Although *Package 2* is good from a thermomechanical reliability perspective, it is not recommended from an electrical performance viewpoint due to the higher electrical parasitics associated with the high-compliant interconnects. Therefore, similar to the case of G-Helix interconnects, for FlexConnects as well *Package 3* represents a judicious trade-off between electrical parasitics and mechanical reliability.

Table 6.5: Estimated Fatigue Life and Failure Location for FlexConnects

Package 1 *Column Interconnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	9.9034
	Predicted $N_{50\%}$	9
	Location of failure	Die Side
Package 2 *High-Compliance FlexConnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	0.2960
	Predicted $N_{50\%}$	2897
	Location of failure	Arcuate Beam
Package 3 *Heterogeneous Interconnects*	$\Delta\varepsilon_{acc,pl}/2$ (%)	0.3026
	Predicted $N_{50\%}$	2792
	Location of failure	Arcuate Beam

6.9 Conclusions

In this chapter, an alternative approach to compliant interconnects utilizing a heterogeneous combination of column-like interconnects near the center of the die and compliant interconnects with increasing level of compliance toward the edge the die is proposed. The modified fabrication process to realize such a heterogeneous combination of interconnects is described. Fabrication results for the heterogeneous interconnects at a 100 μm pitch on a 10 mm x 10 mm die are presented. These heterogeneous array of interconnects appear to provide a balanced combination of mechanical and electrical performance without compromising the thermo-mechanical reliability. Through FEA simulations it was demonstrated that the die stresses induced by the compliant interconnects are an order of magnitude lower than the die stresses in FCOB assemblies, and hence the compliant interconnects are not likely to crack or delaminate low-K dielectric material. Finally, this heterogeneous interconnect concept is shown to be compatible with the FlexConnect design and fabrication process developed in Chapter 4 and Chapter 5 respectively.

CHAPTER 7
ASSEMBLY AND RELIABILITY ASSESSMENT OF COMPLIANT FREE-STANDING INTERCONNECTS

7.1 Introduction

The previous chapters discussed the design and fabrication of compliant interconnects. The design of the compliant interconnect influences its reliability. The fabrication process also influences the reliability of the compliant interconnect as it determines the realizable designs. A third factor that influences the reliability of the interconnect is the assembly process i.e. the process which completes the realization of the mechanical and electrical connection between the die and the substrate. After the fabrication of the compliant interconnect on the wafer, the wafer is singulated into individual dies. The die is then assembled on a substrate and subjected to reliability testing. This chapter focuses on these two aspects – first the assembly process is discussed followed by the reliability assessment of the assembly. For this purpose, both the G-Helix interconnect and parallel-path FlexConnects are considered.

First the unique challenges associated with assembling compliant interconnects are discussed (Section 7.2). This is followed by a description of the assembly of G-Helix interconnects (Section 7.3) and the experimental evaluation of its thermomechanical reliability (Section 7.4). The assembly (Section 7.5) and reliability assessment of parallel-path FlexConnects is then described (Section 7.6). The reliability of parallel-path FlexConnects is also compared against that of single-path FlexConnects (Section 7.6.3).

7.2 Assembly of Compliant Interconnects

Chip assembly is the process of electrically connecting I/O bond pads on the Integrated Circuit (IC) to the corresponding bond pads on the package [Baldwin 2001]. The flip chip assembly has two significant processing steps after the alignment of the

chip to the substrate. As part of the first step the solder bumps on the chip are attached to corresponding pads on the substrate and reflowed above their melting temperature. This forms the mechanical and electrical connection between the die and the substrate. As part of the second step in the assembly process for flip chips, underfill is dispensed between the chip and the substrate, and then cured. This is necessary to ensure the reliability of the solder interconnect. A similar approach can be adopted towards the assembly of compliant interconnects but with two significant differences. First, no underfill material is required for compliant interconnects. Second, the assembly of compliant interconnects introduces some unique challenges when compared to assembly with conventional solder bumps, as the compliant leads can move. Similar to the flip chip process, the assembly of compliant interconnects can be done with solder. A challenge with using solder is ensuring localized wetting of the metal compliant interconnect. In the case of encapsulated interconnects such as Tessera's WAVE (Section 2.4.2) this is not of great concern as the encapsulant protects the solder from wetting the rest of the interconnect. However, for the case of metal interconnects which are exposed, like the G-Helix, Sea of Leads (SoL) interconnects (2.4.4), the solder should not wet the complete interconnect. This would restrict the movement of the interconnect, impairing its ability to be compliant. Another novel aspect of compliant interconnects, especially free-standing interconnects is their compliance in the out-of-plane direction. This allows the interconnects to displace in the out-of-plane direction and hence take up the non-planarity of the substrate and uneven height of the solder bumps. However, to take advantage of this, an out-of-plane force needs to be applied during the assembly process. For conventional solder bump assembly this is not done.

7.3 G-Helix Interconnect Assembly

7.3.1 Test Vehicle Design

The test vehicle design corresponds to a die size of 20 mm x 20 mm. The interconnects on the chip are in a three row peripheral array format at a 100 μm pitch. The substrates on which the chips are assembled have matching pads. The chip has a blanket layer of sputtered Cu on which the interconnects are fabricated. The substrate has a daisy chain structure. The daisy chain structure and the probe pads are designed such that the failure location can be narrowed down to one to few pairs of interconnects. The substrate layout is shown in Figure 7.1. The substrate is a high modulus low CTE (α_{FR-4} = 11 ppm/°C) FR-4 substrate. The large die size and the fine pitch make the alignment of the G-Helix interconnects to the corresponding pad on the substrate challenging for the following reason. As the chip and the substrate have different CTE's, they will expand by different amounts when subjected to a temperature change. Hence, if the chip is aligned to the substrate at room temperature (25°C), when they are taken to the reflow temperature (eutectic SnPb has a reflow temperature of 183°C) they will become misaligned. To minimize this, the pitch of the pads on the substrate is reduced to 99.9μm from 100μm. This results in the chip being aligned to the substrate at a temperature of 150°C.

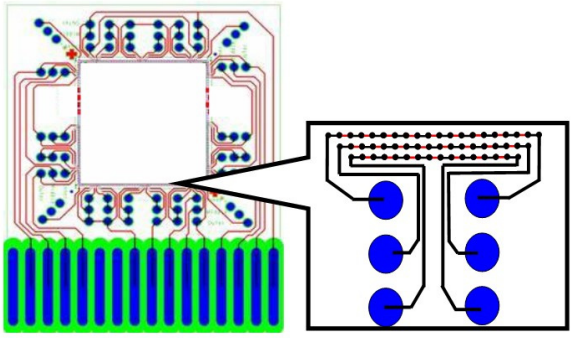


Figure 7.1: Substrate Layout

Assemblies at a fine pitch of a 100μm also require the use of a solder mask material on the substrate. A solder mask is a heat-resisting coating material applied to selected areas of a PWB to prevent the deposition of solder upon those areas during subsequent soldering, and in particular, to prevent solder bridging between conductive pads [Baldwin 2001]. Solder mask also minimizes handling damage during the assembly process. Probimer 81 liquid photoimageable soldermask is the soldermask utilized.

Figure 7.2 illustrates the substrate pad configuration. As seen, the substrate pad is solder-mask defined with a pad opening of 35 – 40 μm in diameter. The thickness of the soldermask is 3 – 4 μm on top of the copper pads. The copper pads have an electroless nickel gold (ENIG) finish. The substrates obtained from a supplier did not have solder on the substrate pads, which is needed for the purpose of assembly. Hence, utilizing a photolithographic process, 60Sn/40Pb solder is electroplated on the copper pads. The electroplating solution used is "Technic Solder Matte NF 820 HS (60/40), Ready To Use solution" and is obtained from Technic Inc. An electroplating setup similar to that described in Figure 5.9 was used. The thickness of the solder plated was approximately 15-20 μm.

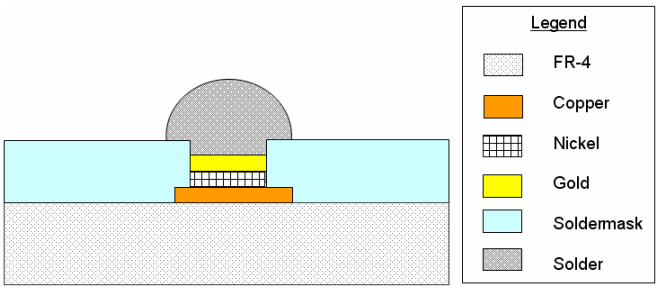


Figure 7.2: Substrate Cross-section with Surface Finish (not to scale)

7.3.2 Interconnect Fabrication for Assembly

For purposes of flip chip assembly on organic substrates, the tip region of the top post of the interconnect should have suitable metallurgy. Accordingly, as described in

Figure A.1(g), a part of the top post of the interconnect is exposed by dry etching the third layer photoresist in a reactive ion etchant. The third layer photoresist is NR9-8000P. The process recipe used to etch the photoresist is the same as described in Section 5.6.2. The appropriate metallurgical interface can then be plated on the exposed copper post. Two metallurgical interfaces were explored in this study. The first choice, as shown in Figure A.1(g2) involved plating a nickel barrier layer followed by 60Sn/40Pb solder plating. The plated solder can then be utilized for assembling the interconnects on the substrate. However, due to reasons discussed later in this chapter, an alternative metallurgical interface was employed. In this alternative approach, after dry etching the third layer photoresist, layers of nickel and gold were plated on the tip of the interconnect, as illustrated in Figure A.1(g1). The gold layer serves as an anti-oxidation barrier layer. The solder is now electroplated or stencil-printed on the substrate pads for the purpose of assembly. The purpose of the current study is to demonstrate the assembly reliability of the compliant interconnects, and therefore, Sn/Pb solder is employed in this work as an electroplating solution for it is readily available.

7.3.3 Assembly Process

Free-standing G-helix interconnects are fabricated on a Si wafer, and the wafer is singulated into 20 mm x 20 mm dies with three-row peripheral-array 100 μm pitch G-Helix interconnects. The dies are then assembled onto substrates.

An RD Automation M10 Flip Chip Bonder (Figure 7.3) is used to perform the assembly. Optical alignment is used to align the chip to the substrate. The flip chip bonder has an optical camera which can look at the bottom of the chip (facing downwards for the purpose of assembly) and at the top of the substrate (facing up for the purpose of assembly). These two images can be superimposed and in this manner the die can be aligned to the substrate. The resolution of the flip chip bonder is ±1μm. Though the bonder does support automatic alignment, manual alignment is used as the image

recognition software needed for automatic alignment is unable to identify features on the substrate. The flip chip bonder can be programmed to apply a variable force and temperature during the assembly process.

Figure 7.3: RD Automation M10 Flip Chip Bonder

Prior to the assembly of the G-Helix interconnects onto organic substrates, the interconnects are assembled onto glass substrates with a stack of sputtered Ti, Cu, and electroplated 60Sn/40Pb layers. Assembly on glass substrates allows for a preliminary optimization of the assembly process as it provides a quick and easy way to inspect the assembly. Figure 7.4 shows the back side of G-Helix interconnects assembled on a glass slide.

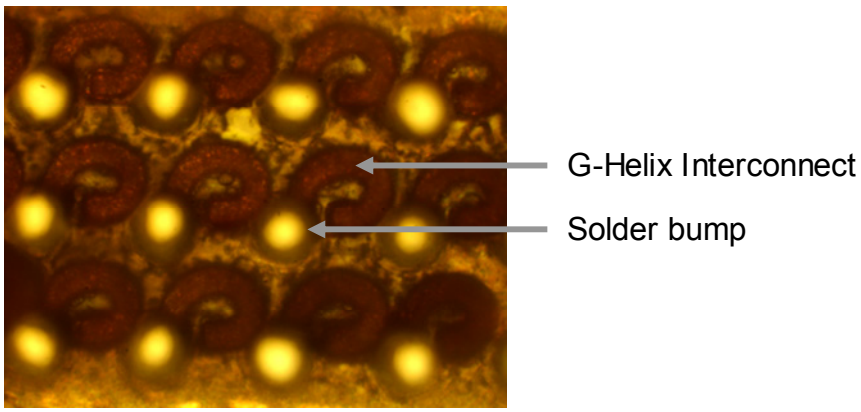


Figure 7.4: Backside of G-Helix Assembly on a Glass Substrate

Critical parameters identified for the assembly process are:

1) Metallurgical Interface: As discussed previously, two different metallurgical interfaces, Ni/SnPb or Ni/Au, can be plated on the tip of the interconnects for the purpose of assembly. Initial assemblies performed utilizing the Ni/SnPb interface resulted in poor yield on assembly. This is believed to be due to the RIE etch of the SU8 photoresist during the release of the interconnects. The RIE process results in excessive oxidation of the solder. This limits the ability of the solder to wet the pads on the substrate. Utilizing a Ni/Au interface with the Au serving as an anti-oxidation barrier results in a significant improvement in assembly yield. Solder for the purposes of assembly in this case is now plated on the substrate pads as described before.

2) Flux Volume: After the alignment of the chip to the substrate, but prior to the attachment of the chip to the substrate, flux is dispensed on the surface of the substrate. Liquid Flux 5RMA supplied by Indium Corporation was used for the purpose of assembly. 5RMA is a mildly activated, no-clean flux. As it is a no-clean flux, removal of the flux after the reflow process is not necessary. The volume of flux was observed to impact assembly yield. On one hand, sufficient flux must be dispensed to reduce the oxides on the surface of the solder and to provide a deoxidized surface for the solder to wet. However, on the other hand, excessive flux would prevent the solder from wetting the interconnects. Therefore, a suitable flux volume is determined during assembly process development.

3) Compressive Force Profile: Free-standing compliant interconnects like G-Helix interconnects have an out-of-plane compliance which allows them to overcome the substrate non-planarity as well as the non-uniformity of the electroplated solder. During the assembly development process, it is seen that the yield on assembly was extremely low when there was a low force (100g or .981N) applied on the backside of the die. However, it is also observed that if a large force (greater than 350g or 3.4335N) was applied it would excessively deform the G-Helix interconnects, causing the arcuate beam

to contact the neighboring pad on the substrate. This in turn would cause the solder from the neighboring pad to wick onto the arcuate beam during reflow resulting in misalignment. Therefore, through process development, a compressive force of 250g (2.4525N) was found to be appropriate to get a good assembly yield. Therefore, all of the assemblies are performed with a 250g (2.4525N) compressive force on the backside of the die as illustrated in Figure 7.5.

4) Temperature Profile: Reflowing solder comprises of having the solder heated up to its melting temperature. The solder is either electroplated or stencil printed onto the PWB, or on the bottom post of the G-Helix. This subsequently creates a connection as the interconnects on the silicon side wet the solder on the PWB at the reflow temperature of solder. The temperature profile used to reflow the solder should be monitored carefully as the reliability of the solder joint is subject in part to the reflow profile used. The temperature profile for solder reflow can be divided into four stages: pre-heat, thermal soak, reflow, and cool down. The pre-heat stage elevates the temperature of the chip and the substrate in a controlled manner. This is followed by the thermal soak stage during which the assembly is held at a constant temperature and / or the temperature is increased at a slow rate. The purpose of the thermal soak stage is to equalize the temperature of all parts of the assembly, as they may not have similar thermal masses. In the next stage, reflow, the assembly is taken above the liquidus temperature of the solder. The assembly is generally taken to a temperature which is about 20°C to 25°C above the liquidus to ensure that sufficient fluxing action and wetting of the solder. Increasing the temperature above this and / or keeping the assembly above the liquidus temperature is not advisable as it results in the formation of harmful intermetallics which detrimentally impact interconnect reliability. The final stage, the cool down of the assembly, must be done in a controlled manner, preferably at a rate which is lower than 4°C/min. Each of the four stages must be optimized as it impacts assembly yield as well the subsequent reliability of the solder joint.

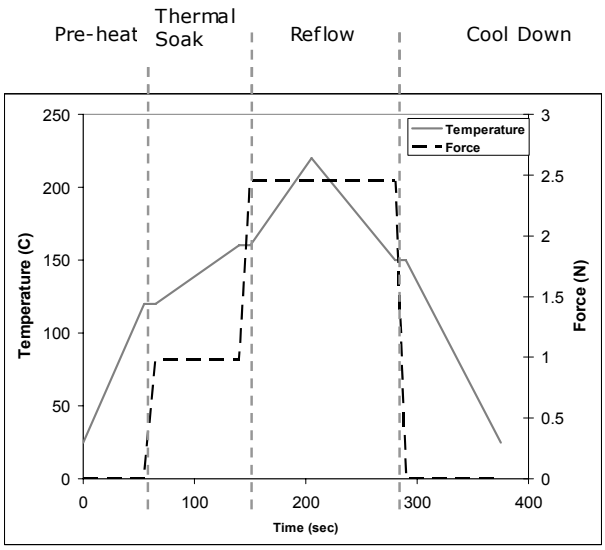


Figure 7.5: Approximate Assembly Force and Temperature Profile for Assembly of G-Helix Interconnects

The optimized force and temperature profile is shown in Figure 7.5. As seen, after the pre-heat stage a minimal amount of force (100g or .981N) is applied to bring the die in contact with the substrate. This is followed by a thermal soak stage (from 120°C to 150°C), at the end of which, the determined optimized force (250g or 2.4525N) to overcome the non-planarity is applied. This force is maintained during the subsequent solder reflow stage. This is followed by the cool down stage, at the beginning of which the applied force is released.

Using the developed assembly process, chips were assembled on an organic substrate. This is shown in Figure 7.6. To verify the alignment of the assembly X-ray inspection was performed. The X-ray inspection equipment generates a grayscale image with darker images being produced for structures that are thicker or materials that are denser. For the assembly performed the X-ray images are shown in Figure 7.7. The figure shows an X-ray image of the full chip with magnified views of each corner of the assembly. In the magnified images, the pads on the substrate can be seen as well as two

posts of the G-Helix interconnect. Based on the images the alignment of the assembly is good.

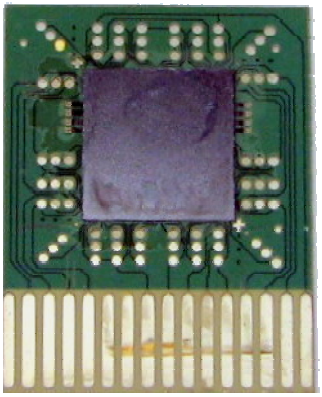


Figure 7.6: Chip with G-Helix Interconnects Assembled on Organic Substrate

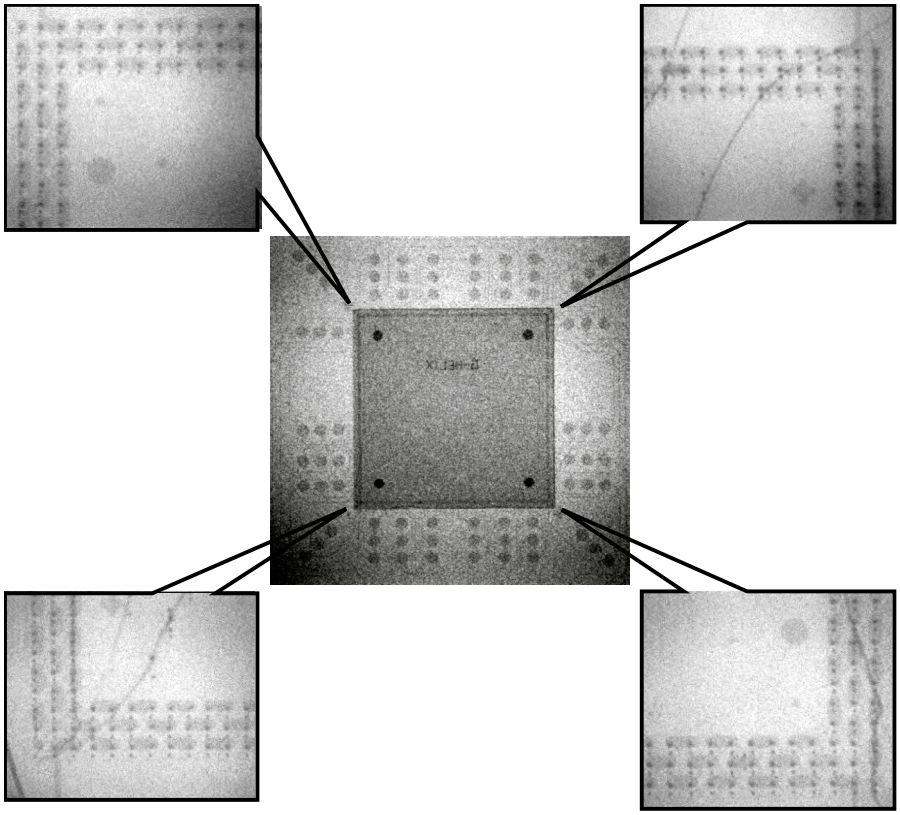


Figure 7.7: X-Ray Image of G-Helix Interconnects Assembled on Organic Substrate

A cross-section of the assembled G-Helix interconnect on an organic substrate is shown in Figure 7.8. As seen, the solder only wets the tip of the interconnect as it has a

Ni/Au layer. The remaining surface of the interconnect is not wetted by the solder as it has a thin layer of copper oxide.

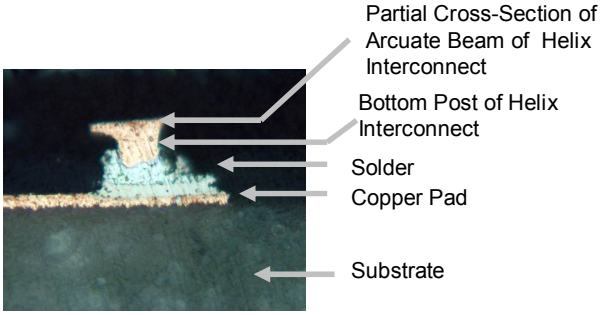


Figure 7.8: Cross-Section of G-Helix Interconnect Assembled on an Organic Substrate

Using the developed assembly process, four test vehicles were assembled on organic substrates for reliability testing. Out of the four assembled samples, three test vehicles provided 100% assembly yield, while one test vehicle provided 55% assembly yield due to poorly-defined pad openings on the substrate.

7.4 Reliability Assessment

The reliability of a packaged microelectronic system is defined as the probability that this system will be operational within acceptable limits for a given period of time [Qu and Guo 2001]. For typical field-use conditions the reliability of microelectronic packages would extend over several years. As tests cannot be performed over such time scales, they need to be accelerated. The accelerated tests are then correlated to field-use conditions through an acceleration factor. Failure in a microelectronic system is normally seen at the system level – for example, a computer that does not boot up. Failure modes however, are seen at the component level. Failure mechanisms can be chemical, physical, thermomechanical or electrical.

A primary concern with compliant interconnects is their thermomechanical reliability. Electronic packages employ a wide variety of materials with differing material properties and more specifically differing CTE's. Hence, when these assemblies

experience a change of temperature, strains and consequently stresses are developed. For the case of first level interconnects there exist a CTE mismatch between the silicon die and the organic substrate. The silicon die has a CTE of around 3ppm/°C whereas an organic substrate has a CTE of around 11-17 ppm/°C. Compliant interconnects attempt to accommodate this CTE mismatch and as a consequence experience failure due to low-cycle fatigue. To evaluate the thermomechanical reliability of an assembled compliant interconnect, they are subjected to a thermal-cycling test. As part of the thermal-cycling test the assembly is cycled between two temperature extremes. A thermal-cycling test is characterized by the two temperature extremes, the ramp rate or the time taken to go from one temperature extreme to another, and the time for which the assembly is held at the elevated temperature also referred to as the dwell time.

7.4.1 Reliability Assessment of G-Helix Interconnects

A thermal-cycling test specified by the Joint Electron Devices Engineering Council (JEDEC) is used to evaluate the thermo-mechanical reliability of the G-Helix assembly. The G-Helix interconnects assembled on organic substrate were subjected to JEDEC (JESD22-A104-B), test condition J thermal profile – cycling between 0 and 100 °C with 10 minute dwell times [JEDEC 2000].

The assemblies are taken out at regular intervals during thermal cycling and the daisy chain resistance is measured. As the test vehicles contained several individual daisy chains, rather than one loop for all interconnects, all of the test vehicles are used in the thermal cycling experiments, and the electrical resistance of various daisy chains is monitored through thermal cycling. The daisy chain resistance is typically measured to have a value between 1Ω and 3 Ω when functional. An open circuit was determined as the criteria for failure. The thermal cycling results for each of the assemblies are presented in Figure 7.8. The vertical axis correspond to the number of working probing pads calculated as a percentage of the number of working probing pads after assembly

but prior to thermal cycling. As seen for all four assemblies some of the interconnects are seen to work beyond 1000 thermal cycles. However, sample 4 demonstrates the best reliability with over 95% of the pads lasting 422 thermal cycles. The variation between the reliability of the different samples is due to variability in the assembly process introduced by the non-uniform openings defined in the solder mask of the substrate. The failure mode for the first three assembled samples (sample 1, sample 2, sample 3) after the thermal cycling tests is observed to be cracking in the solder joints which connect the interconnects to the substrate. This is illustrated in Figure 7.10 in which a cross-section of a failed interconnect is shown. The crack in the solder joint may have been exaggerated by the molding process which is required to obtain the cross-section image. However for sample 4, apart from failure in the solder joint an additional failure mode is observed in which the interconnect fails in the arcuate beam. This is illustrated in the SEM shown in Figure 7.11 and the video microscope images shown in Figure 7.12. To obtain this images the die was removed the substrate. This failure location is close to the failure location predicted by FEA models, and shown in Figure 6.8. This sample also exhibits the best reliability which would indicate that the quality of the assembly process is superior to the other samples.

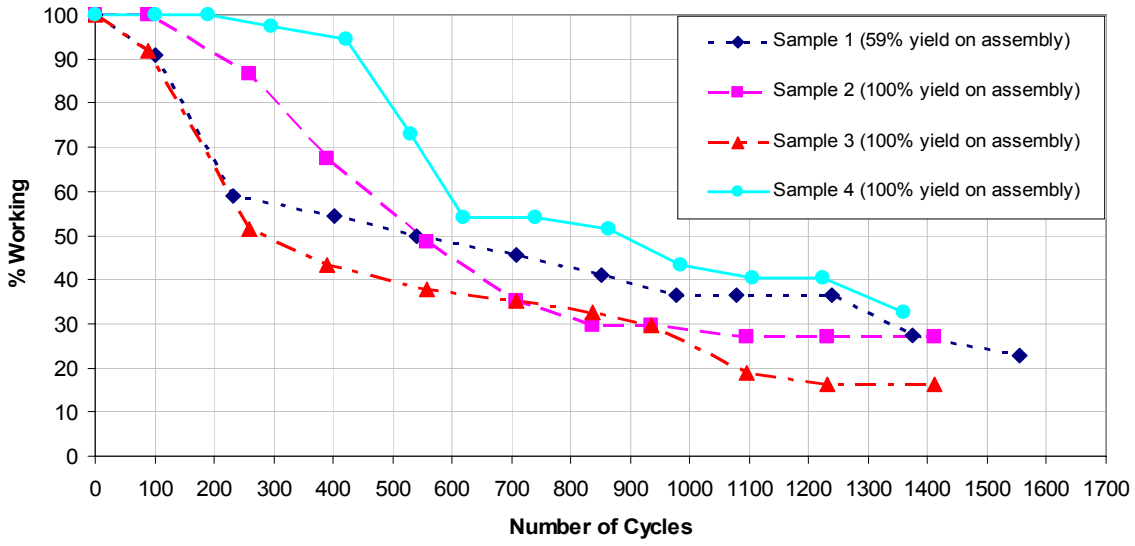


Figure 7.9: Failure Data for G-Helix Interconnects

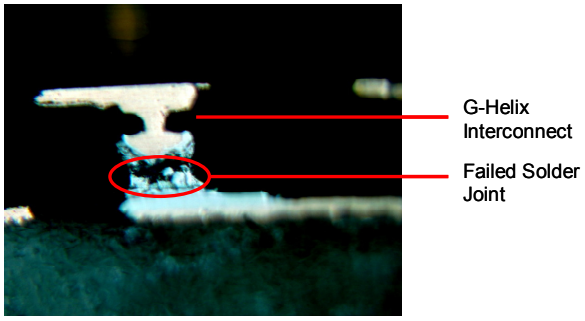


Figure 7.10: Cross-Section of Failed Solder Joint for G-Helix Interconnect

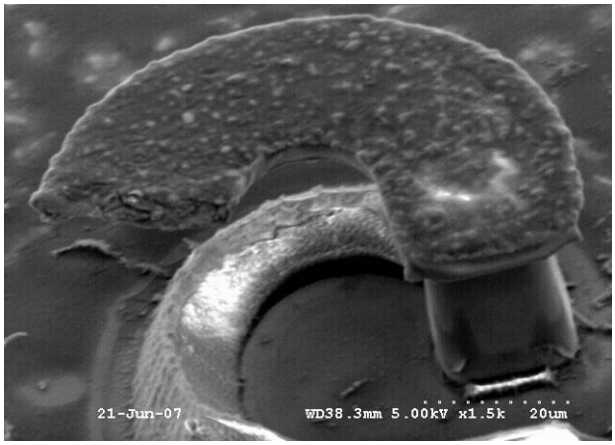
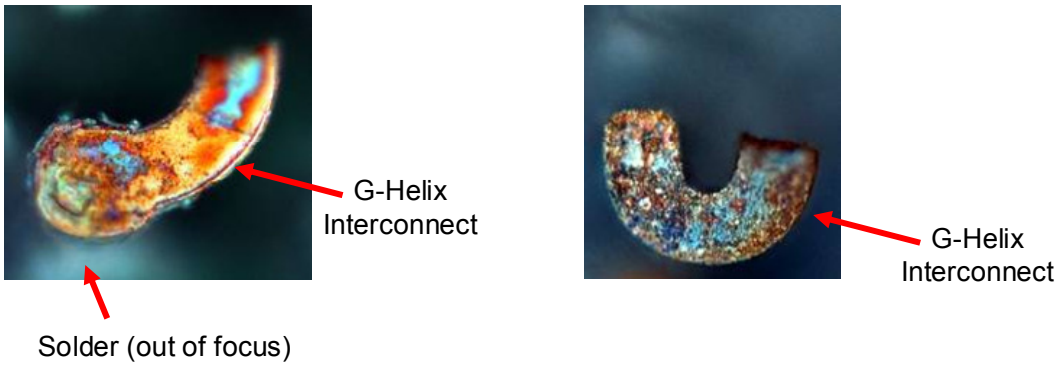


Figure 7.11: SEM Image of Failed G-Helix Interconnect for Sample 4



(a) Substrate Side (b) Die Side

Figure 7.12: Video Microscope Image of Failed G-Helix Interconnect for Sample 4

7.5 FlexConnects Assembly

7.5.1 Test Vehicle Design

The die side test-vehicle design used to assemble parallel-path FlexConnects is described in Section 5.5 of this dissertation. The organic substrates used for the assembly of FlexConnects are identical to those used for G-Helix interconnects and are described in Section 7.3.1 of this dissertation. The substrate pad pitch, as before, was 99.9 μm. Similar to the G-Helix interconnects, solder for the purpose of assembly is plated on the substrate.

7.5.2 Localized Reflow of Solder for FlexConnects

For the case of G-Helix interconnects solder wetting is localized to the tip of the interconnect due to the deposition of a thin wettable layer of Ni/Au at the tip of the interconnect and the presence of a relatively non-wettable layer of copper oxide along the rest of the interconnect. For the case of parallel-path FlexConnects an alternate approach was adopted. The geometry of the interconnect is defined in a manner that restricted the solder to the circular pad shown in Figure 4.4. The transition from the relatively narrow beam to the wide circular pad ensures localized wetting due to surface tension effects. This is because the planar dimensions of the circular pad are larger than that of the beam.

Hence, to minimize the surface energy during reflow, the volume of solder and consequently the thickness of the solder will be greater on the circular pad as compared to the neck. Therefore, it is energetically not favorable for the solder to wet the arcuate beam. Solder should not wet the remaining arcuate structure, as such a wetting would detrimentally impact the compliance of the interconnect structure. A similar concept has been utilized previously for wafer-level packaging and is described in [Rinne et al. 2000].

An experiment was conducted to verify this. Using only the second layer mask (Figure 5.4), by photolithographic processes a stack of uniform thickness is electroplated with the parallel-path FlexConnect geometry. The stack is plated on a seed layer of Ti/Cu that is sputtered on a silicon wafer. The plated stack consisted of an initial layer of copper, an intermediate thin layer of nickel/gold and a final layer of solder (as the structure is directly plated on the surface of the silicon wafer, it is not compliant). The copper layer is approx 4 μm thick, the Ni/Au layer is approx 1 μm thick and the solder layer is approx 4 μm thick. This is then reflowed and it is observed that the solder wicks towards the circular pad. This is shown in Figure 7.13. In other words, due to surface tension effects, the solder becomes thicker on the circular pad and thinner on the arcuate beam. Hence, based on this experiment, it is expected that when parallel-path FlexConnects are assembled, the solder would preferentially wet the circular pad.

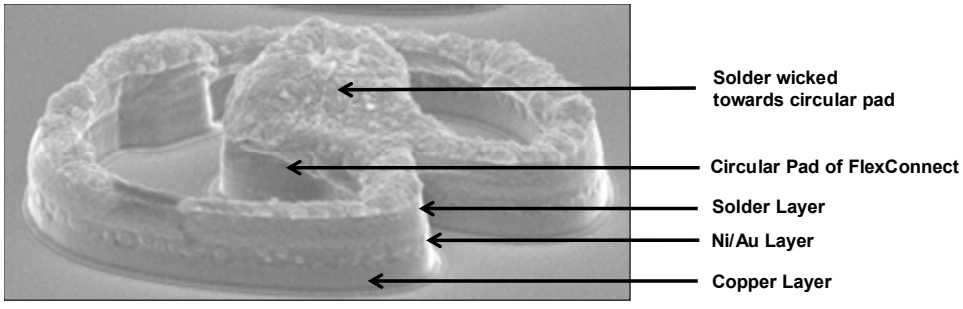


Figure 7.13: Solder Wicking towards Circular Pad of FlexConnect

7.5.3 Assembly Process

Free-standing parallel-path FlexConnects are fabricated on a Si wafer, and the wafer is singulated into 20 mm x 20 mm dies with three-row peripheral-array 100 µm pitch parallel-path FlexConnects. The dies are then assembled onto substrates. Again, an RD Automation M10 Flip Chip Bonder is used to perform the assembly. The alignment for assembly is performed manually.

Prior to the assembly of the parallel-path FlexConnects onto organic substrates, the interconnects are assembled onto glass substrates with a stack of sputtered Ti, Cu, and electroplated 60Sn/40Pb layers. Assembly on glass substrates is used to perform a preliminary optimization of the assembly process. Parallel-path FlexConnects assembled on a glass substrate are shown in Figure 7.14.

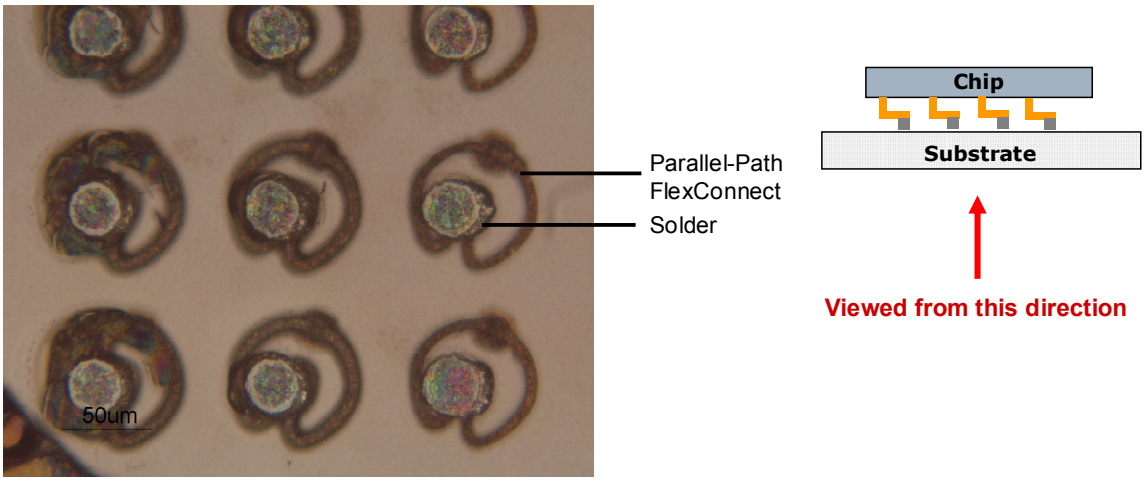


Figure 7.14: Backside of FlexConnect Assembly on a Glass Substrate

The temperature and force profile used for the assembly process of parallel-path FlexConnects is similar to that utilized for G-Helix interconnects. The peak force used during the assembly process is modified for FlexConnects as its out-of-plane compliance and stand-off height is lesser than that of G-Helix interconnects. The optimal force was determined to be 300g. Figure 7.15 shows a chip with parallel-path FlexConnects which

are assembled on a glass substrate and then sheared off the glass substrate. The solder is seen to locally wet the parallel-path FlexConnect only in the region of the circular pad, validating the use of this approach to cause localized wetting. In addition, when the chip is sheared off the substrate, failure is observed in the bulk of the solder joint. This indicates that the solder wets the interconnect well, as the copper interconnect to solder joint interface does not fail.

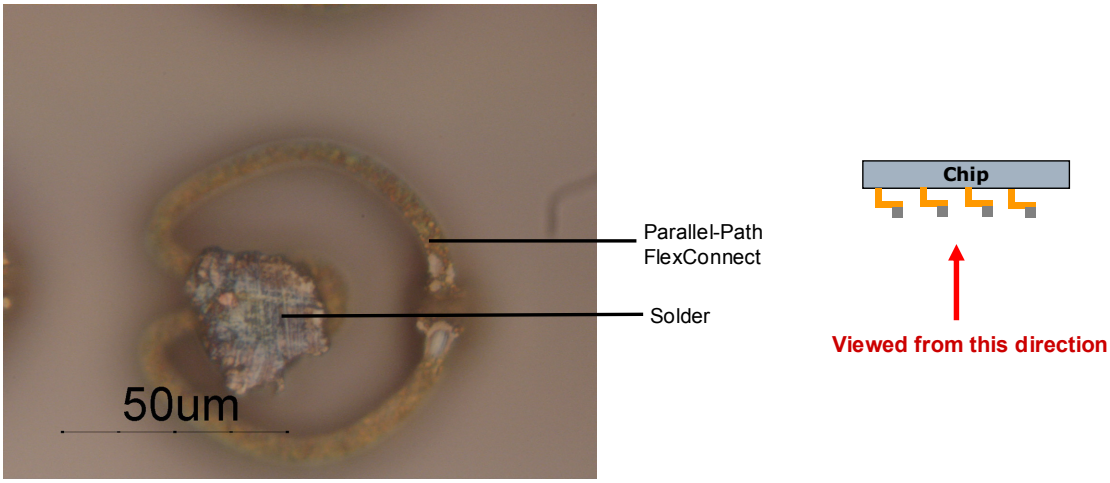


Figure 7.15: Chip with FlexConnect Sheared Off Glass Substrate

Using the developed assembly process, one test vehicles is assembled on an organic substrate for reliability testing. The yield on assembly was 52%.

7.6 Reliability Assessment of FlexConnects

7.6.1 Experimental Reliability Assessment of Parallel-Path FlexConnects

The parallel-path FlexConnects assembled on organic substrate are subjected to JEDEC (JESD22-A104-B), test condition J thermal profile – cycling between 0 and 100 °C with 10 minute dwell times [JEDEC 2000].

The assemblies are taken out at regular intervals during thermal cycling and the daisy chain resistance is measured. The test vehicle contained several individual daisy chains which allowed for localization of the failure location. An open circuit was determined as the criteria for failure.

After 71 thermal cycles, 65% of the pads are working (calculated as a percentage of initially working pads). After 143 cycles, none of the pads are working. The approximate failure location on the chip is shown in Figure 7.16. Also are shown video microscope images at three different locations around the chip. These images are obtained by shearing the chip off the substrate and taking images of the substrate. The failure location when this is done is at the interface between the parallel-path FlexConnect and the silicon chip. Based on these images, two reasons can be postulated for the premature failure of the interconnects. The first is the misalignment introduced by the assembly process. For the image corresponding to the bottom left corner of the chip the vertical post of the interconnect is assembled onto the solder on the substrate (instead of the circular pad being assembled on the solder) and hence the interconnect has minimal compliance. Therefore, it most likely failed during the cool down from reflow. For the image corresponding to the bottom right corner of the chip the misalignment is not as severe and hence the interconnect does not fail during the reflow process. However, the compliance is still reduced and causes the interconnect to fail prematurely. The misalignment can be corrected by properly calibrating the assembly equipment. However, the second cause for the premature failure, corresponding to the top right image of Figure 7.16, is of greater concern. In this case, the alignment is better, however, due to the large diameter of the openings in the solder mask, the solder wets a large part of the interconnect restricting its compliance. Therefore, even if the chip is properly aligned to the substrate, the second problem would still remain. Substrates with a smaller diameter opening in the solder mask are not available. In conclusion, due to limitations of the test vehicle substrate, it is not possible to evaluate the experimental thermomechanical reliability of the parallel-path FlexConnects.

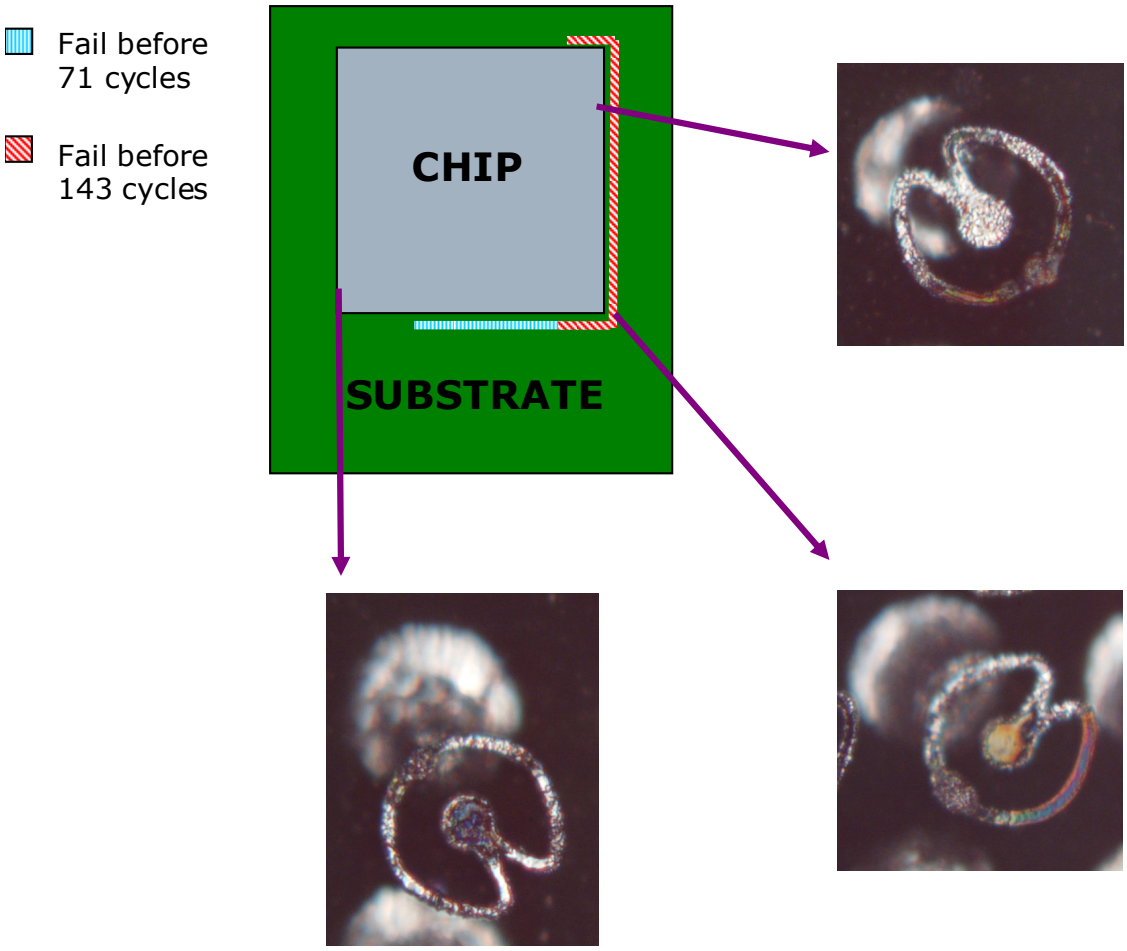


Figure 7.16: FlexConnects Failure Location

7.6.2 Virtual Reliability Assessment of Parallel-Path FlexConnects

As it is not possible to assess the thermomechanical reliability of FlexConnects experimentally, an alternate approach was adopted. A popular approach used for the evaluation of the thermomechanical reliability of interconnects is to develop finite element models representing the interconnects as part of an electronic package. The parallel-path FlexConnects studied are identical to the interconnects fabricated in Chapter 5 of this dissertation. A GPD model (Figure 7.17) is developed representing the following: a 20 mm x 20 mm silicon die, a single peripheral row of 100 µm-pitch parallel-path FlexConnects, solder attach, copper pad, and a 30 mm × 30 mm organic FR-4 substrate. The meshed GPD model is shown in Figure 7.18.

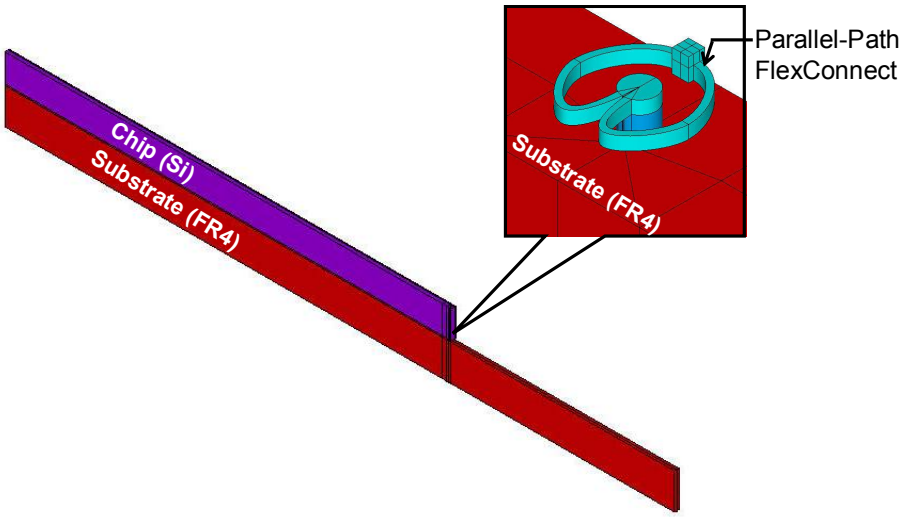


Figure 7.17: Schematic Representation of GPD Model of WLP with Parallel-Path FlexConnects

The material models are identical to those used for the GPD model developed in Section 6.6. In the finite-element model, the copper parallel-path FlexConnects is modeled as a temperature-dependent multi-linear kinematic hardening material [Iannuzzelli 1991]. Silicon is modeled as isotropic, linear elastic and temperature dependent. The organic substrate is modeled as orthotropic, linear elastic and temperature dependent. The solder is modeled as viscoplastic [Wang et al. 2001].

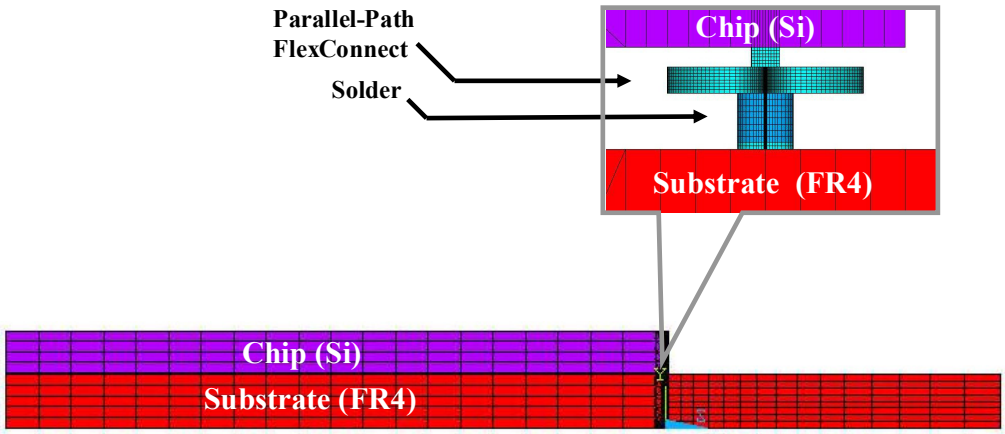


Figure 7.18: Meshed GPD Model of WLP with Parallel-Path FlexConnects

Symmetry conditions are applied along the *x*–symmetry plane. For both the *z*-faces, nodes were coupled in deformation along *z* axis. Also, the left bottom corner of the assembly was fully constrained to prevent rigid body motion. These boundary conditions are illustrated in Figure 7.19.

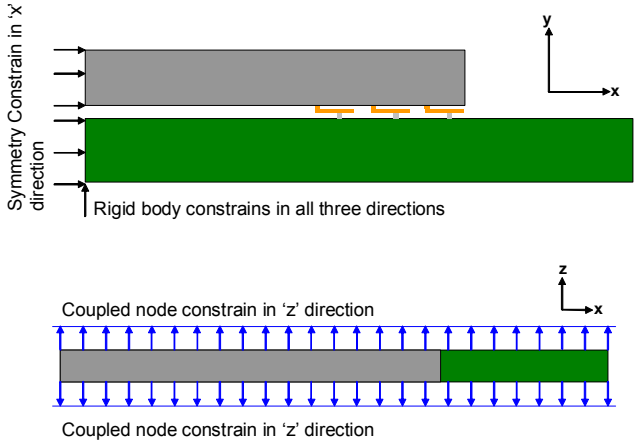


Figure 7.19: GPD Model Boundary Conditions

The thermal loading was simulated as follows: The package is first subjected to a load step from solder melting temperature to room temperature (20°C); it is then dwelled for about an hour at room temperature. Next, the package is subjected to accelerated thermal cycles between 0°C and 100°C with five minute dwells. The stress-strain behavior stabilized after three cycles, and therefore, the results from the third cycle are used for further analysis. A Coffin-Manson-type equation (Equation 6.3) is used to determine the fatigue life of the compliant interconnects.

From the plastic strain component in various parts of the assembly, the fatigue life of the parallel-path FlexConnect as well as the solder joint is determined, and it is found that the parallel-path FlexConnect was likely to fail first compared to the solder joint, as intended in the design.

The accumulated plastic strain distribution for the parallel-path FlexConnects interconnect from the third "stabilized" thermal cycle is shown in Figure 7.20.

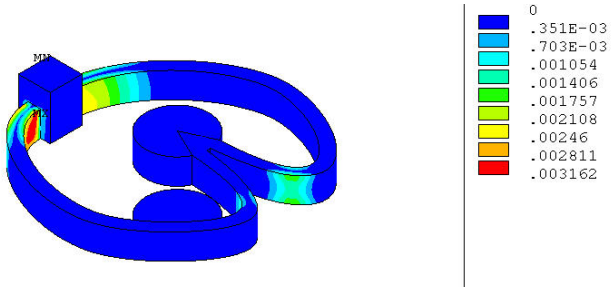


Figure 7.20: Accumulated Plastic Strain Over 3rd Thermal Cycle for Parallel-Path FlexConnects

Based on Equation 6.3, the estimated fatigue life of the parallel-path FlexConnects with the accumulated plastic strain is provided in Table 7.1. A similar analysis for an equivalent G-Helix interconnect package has been performed. Like the parallel-path FlexConnects the G-Helix interconnect package was subjected to thermal cycling between 0°C and 100°C with five minute dwells. To ensure a valid comparison between the two interconnect designs the number of elements across the width of the arcuate beam was kept the same. The direction in which the strain gradient is maximum is across the width of the beam and it is in the arcuate beam that failure is observed in both cases. These results are also summarized in Table 7.1. Based on these results it is expected that the fatigue behavior of parallel-path FlexConnects would be comparable to that of G-Helix interconnects which have been experimentally shown to last in excess of a 1000 thermal cycles. However, the electrical performance of parallel-path FlexConnects is superior to G-Helix interconnects and the fabrication process for realizing parallel-path FlexConnects is simpler and hence more cost effective. The parallel-path FlexConnects design is also redundant.

To highlight the redundancy of the parallel-path FlexConnect a GPD model was developed in which one path of the parallel-path FlexConnect is removed. Apart from this, the GPD model is identical in all respects to the GPD model previously described. This model represents the scenario in which one of the arcuate beams has failed and the interconnect continues to provide an electrical path through the second arcuate beam

which has not fatigue failed. When the fatigue life of the parallel-path FlexConnect with one path removed is evaluated, the $N_{50\%}$ life is found to be equal to 2716 cycles (177% increase). This illustrates the advantage of the redundant design of the interconnect as the fatigue life of the interconnect will increase once one of the arcuate beams fail. However, this is at the expense of the electrical performance of the interconnect. Simulations are conducted in FastHenry to evaluate the DC inductance and resistance of a parallel-path FlexConnect in which one of the arcuate beams has failed. The inductance and resistance increase significantly. The inductance is found to be 63.31pH (71% increase) and the resistance is found to be 76.90mΩ (88% increase).

Table 7.1: Estimated Fatigue Life of Parallel-Path FlexConnect and G-Helix Interconnect

	$\Delta\varepsilon_{acc,pl}/2$ (%)	Predicted $N_{50\%}$	Location of failure
Parallel-Path FlexConnects Package	0.5668	981	Arcuate Beam
G-Helix Package	0.5926	911	Arcuate Beam

7.6.3 Virtual Reliability Assessment of Single-Path FlexConnects

To illustrate the advantage of using multiple paths as part of a compliant interconnect design from a thermomechanical reliability perspective a finite element model is developed representing a single path FlexConnects. The GPD finite element model developed (Figure 7.21) is identical in all aspects to the GPD model developed in Section 7.6.2, apart from the interconnect design. The arcuate beam of the single-path FlexConnect has an 8 μm x 8 μm cross-section and identical radius of curvature as the parallel-path FlexConnect. Each of the arcuate beams of the parallel-path FlexConnect have an 8μm (thickness) X 4μm (width) cross-section i.e. the total cross-sectional area for both beams combined is the same as that of the single-path FlexConnect. The meshed GPD model for single-path FlexConnects is shown in Figure 7.22.

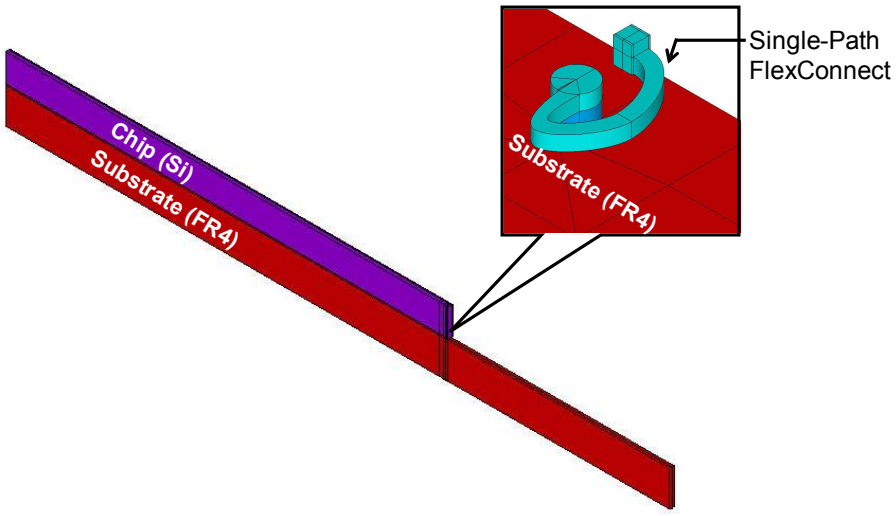


Figure 7.21: Schematic Representation of GPD Model of WLP with Single-Path FlexConnects

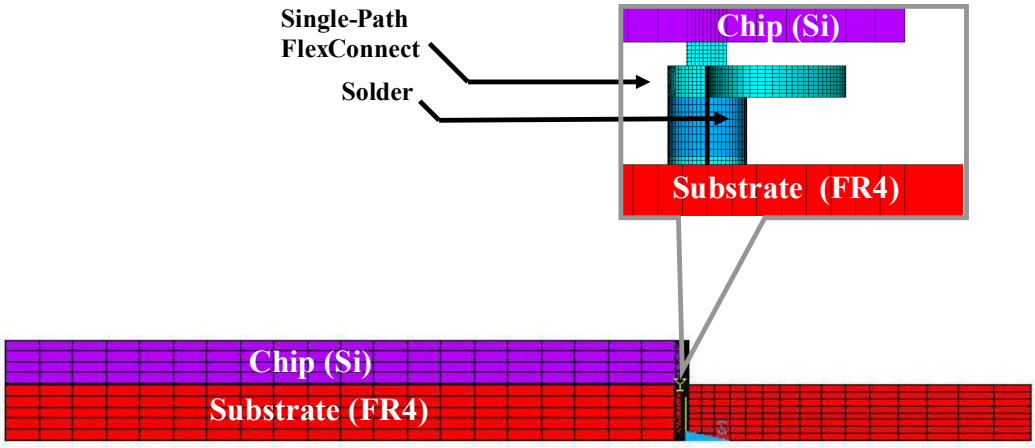


Figure 7.22: Meshed GPD Model of WLP with Single-Path FlexConnects

An approach identical to that used for parallel-path FlexConnects is adopted to evaluate the fatigue life of the single-path FlexConnect. To ensure a valid comparison between the two interconnect designs the number of elements across the width of the arcuate beam is kept the same. Again, the stress-strain behavior stabilized after three cycles, and therefore, the results from the third cycle are used for further analysis. From the plastic strain component in various parts of the assembly, the fatigue life of the

single-path FlexConnect as well as the solder joint is determined, and it was found that the single-path FlexConnect is likely to fail first.

The accumulated plastic strain distribution for the single-path FlexConnects interconnect from the third "stabilized" thermal cycle is shown in Figure 7.23.

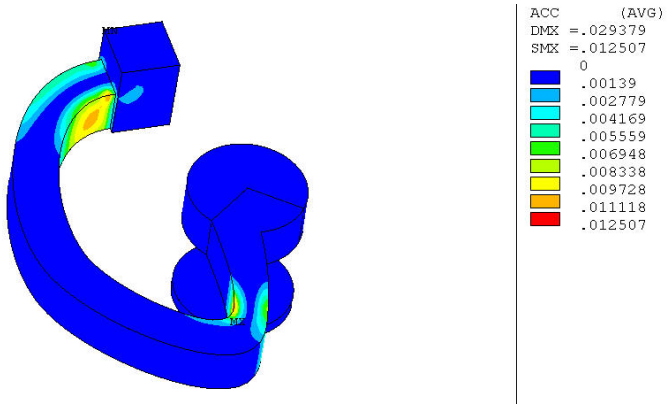


Figure 7.23: Accumulated Plastic Strain Over 3rd Thermal Cycle for Single-Path FlexConnect

Based on Equation 6.3, the estimated fatigue life of the single-path FlexConnects with the accumulated plastic strain is provided in Table 7.2. The estimated fatigue life of an equivalent parallel-path FlexConnect is also provided in the table. Based on these results it is expected that the fatigue life of parallel-path FlexConnects is an order of magnitude greater to that of the single-path FlexConnects, clearly demonstrating the advantage of using multiple electrical paths as part of the interconnect design. The single-path FlexConnects would have a compliance which is approximately $1/4^{th}$ that of the parallel-path FlexConnect. However, due to the non-linear relationship between fatigue life and strain, the fatigue life of the single-path FlexConnect is nearly $1/10^{th}$ that of the parallel-path FlexConnect. The G-Helix interconnect, which also employs a single electrical path, has a higher fatigue life when compared to the single-path FlexConnect. This is because it has a much higher stand-off height. However, the higher stand-off height of a G-Helix interconnect results in a more involved fabrication process.

Table 7.2: Estimated Fatigue Life of Single-Path FlexConnect and Parallel-Path FlexConnect

	$\Delta\varepsilon_{acc,pl}/2$ (%)	Predicted $N_{50\%}$	Location of failure
Single-Path FlexConnects Package	2.5129	82	Arcuate Beam
Parallel-Path FlexConnects Package	0.5668	981	Arcuate Beam

7.7 Conclusion

In this chapter, the assembly and reliability assessment of free-standing compliant interconnects is discussed with the G-Helix interconnects and FlexConnects being considered. G-Helix interconnects at a 100 μm pitch are fabricated on a silicon wafer, and the silicon wafer is singulated to form individual dies. The dies are assembled on glass as well as organic substrates. Critical factors which impact yield on assembly are determined. A yield on assembly of a 100% was achieved. Experimental thermal cycling with a 20 mm x 20 mm die assembled on organic substrates shows that 30% will survive 1000 thermal cycles. For one particular sample, 95% are seen to survive 422 cycles. An assembly process is also developed for the parallel-path FlexConnects, which are assembled on both organic and glass substrates. Localized reflow of the solder at the circular pad of the interconnect was achieved. However, due to limitations of the organic substrate used for assembly, it is not possible to demonstrate the experimental reliability of parallel-path FlexConnects. Hence, an alternate approach based on numerical simulations is used to determine the thermomechanical reliability of parallel-path FlexConnects. For parallel-path FlexConnects at a 100 μm pitch and a 20 mm X 20 mm

die size, the numerical simulations predict that the interconnects will last close to a 1000 cycles. Identical simulations performed for the G-Helix interconnects indicate a similar fatigue life. As the dimensions and the materials used to fabricate / assemble parallel-path FlexConnects are similar to G-Helix interconnects, we would expect the parallel-path FlexConnects to display similar experimental thermomechanical reliability as the G-Helix interconnects. However, the electrical performance of parallel-path FlexConnects is superior to G-Helix interconnects and the fabrication process for realizing parallel-path FlexConnects is simpler and hence more cost effective. In addition the parallel-path FlexConnects design is redundant. The advantage of the redundant design of the parallel-path FlexConnect is shown. However, once one of the arcuate beams fails, the electrical performance of the interconnect degrades. However, the interconnect continues to provide an electrical path through the arcuate beam that has not fatigue failed. Finally, equivalent simulations are performed to compare the thermomechanical reliability of single-path FlexComments (same beam cross-section area as parallel-path FlexConnects) against parallel-path FlexConnects. It is seen that the $N_{50\%}$ life of the single-path FlexConnects was $1/10^{th}$ that of the parallel-path FlexConnects, highlighting the advantage of using multiple electrical paths as part of the compliant interconnect design.

CHAPTER 8
SUMMARY AND CONTRIBUTIONS

8.1 Summary

There are several design, fabrication, assembly, and integration research challenges and gaps with the existing suite of compliant interconnects. FlexConnects, a novel compliant interconnect technology, was developed to address these limitation by innovating on the design of the interconnects at the level of an individual interconnect and at the system level, and by developing a novel cost-effective fabrication process. A comprehensive study was conducted which evaluated the electrical and mechanical performance of the interconnects, optimized the fabrication process to achieve high fabrication yield, identified critical parameters which impact assembly yield and assessed the reliability of free-standing compliant interconnects.

A significant limitation of compliant interconnects is their inferior electrical performance compared to conventional solder bumps. Though the design of the compliant interconnect can be modified to improve its electrical performance, this is generally at the expense of the mechanical performance of the interconnect and hence is not acceptable. To overcome this, a novel design concept is proposed which involves utilizing multiple electrical paths as part of the compliant interconnect design. Through an analytical model it is shown that such an approach improves electrical performance without compromising on mechanical performance. An additional benefit of utilizing multiple electrical paths is that the design is redundant, allowing the interconnect to continue functioning even if one of the electrical path fails. One of the simplest interpretations of this concept based on using multiple columns is shown to have a minimal advantage as compared to a single column for interconnects at a fine pitch. Hence, the multiple electrical paths must lie in the in-plane direction and not in the out-of-plane direction. FlexConnects, a new compliant interconnect, is then developed which incorporates this concept of using multiple electrical paths. Using numerical models the

parallel-path FlexConnect is compared against a single-path FlexConnect. The parallel-path FlexConnect are shown to have a higher mechanical compliance than the single-path FlexConnect and reduced inductance. In other words, by utilizing multiple electrical paths, the mechanical performance and the electrical performance are increased at the same time. Significantly, the parallel-path FlexConnect is a compliant interconnect with a low value of inductance (36.5 pH) as well as sufficient compliance. As a reference the G-Helix interconnect has an inductance of 89 pH [Zhu 2003] and solder bumps have an inductance between 20-25 pH [Kim et al. 2003]. The generic nature of the multiple electrical path concept is shown by applying it to the case of the Sea of Leads interconnect. For the Sea of Leads interconnect when two interconnect paths are utilized, the in-plane mechanical compliance increases by 240% and the out-of-plane compliance increases by 20%. High frequency modeling of the inductance and resistance of the parallel-path FlexConnect is also performed. Skin-effect results in the resistance of the interconnect increasing after 1GHz. The inductance of the interconnect starts decreasing above 100 MHz. The mutual inductance of parallel-path FlexConnects at a 100μm pitch is also calculated. The capacitance of parallel-path FlexConnects is also determined and is shown to be negligible.

A novel and cost-effective MEMS-based process is developed to fabricate the parallel-path FlexConnect design. A sacrificial layer fabrication process, with up to two masking steps is utilized. Such an approach potentially reduces the cost of fabricating compliant interconnects. The approach is implemented to fabricate parallel-path FlexConnects at a 100 μm pitch in a three-row peripheral array format for a 20 mm x 20 mm die size. The fabrication process parameters are optimized and the fabrication process had excellent yield across a 4 inch wafer with interconnects that are uniform and repeatable. Although in this work only a peripheral array of interconnects are realized, the fabrication process can easily be implemented to realize FlexConnects at a 100 μm pitch in a full area-array format.

An additional approach for improving the electrical performance of the complaint interconnects is proposed. This concept utilizes a heterogeneous combination of column-like interconnects near the center of the die and compliant interconnects with increasing level of compliance toward the edge the die. The modified fabrication process to realize such a heterogeneous combination of interconnects is described with G-Helix interconnects considered as a test case. Fabrication results for the heterogeneous interconnects at a 100 μm pitch in an area-array format on a 10 mm X 10 mm die are presented. Through numerical models it is shown that these heterogeneous array of interconnects appear to provide a balanced combination of mechanical and electrical performance without compromising the thermomechanical reliability. Through FEA simulations it is also demonstrated that the die stresses induced by the compliant interconnects are an order of magnitude lower than the die stresses in FCOB assemblies, and hence the compliant interconnects are not likely to crack or delaminate low-K dielectric material. The heterogeneous interconnect concept is then implemented for the case of parallel-path FlexConnect.

Following this, the assembly and reliability assessment of free-standing compliant interconnects are discussed with the G-Helix interconnects and FlexConnects being considered. G-Helix interconnects at a 100 μm pitch were fabricated on a silicon wafer, and the silicon wafer was singulated to form individual dies. The dies were assembled on glass as well as organic substrates. Critical factors which impact yield on assembly were determined. A yield on assembly of a 100% was achieved. Experimental thermal cycling with a 20 mm x 20 mm die assembled on organic substrates shows that 30% will survive 1000 thermal cycles. For one particular sample, 95% were seen to survive 422 cycles. An assembly process was also developed for the parallel-path FlexConnects, which were assembled on both glass and organic substrates. Localized reflow of the solder at the circular pad of the interconnect was achieved. However, due to limitations of the organic substrate used for assembly, it was not possible to demonstrate the experimental

reliability of parallel-path FlexConnects. Hence, an alternate approach based on numerical simulations was used to assess the thermomechanical reliability of parallel-path FlexConnects. For parallel-path FlexConnects at a 100 μm pitch and a 20 mm x 20 mm die size, the numerical simulations predict that the interconnects will last close to a 1000 cycles. Identical simulations performed for the G-Helix interconnects indicate a similar fatigue life for G-Helix interconnects. As the dimensions and the materials used to fabricate / assemble parallel-path FlexConnects are similar to G-Helix interconnects, we would expect the parallel-path FlexConnects to display similar experimental thermomechanical reliability as the G-Helix interconnects. However, the electrical performance of parallel-path FlexConnects is superior to G-Helix interconnects and the fabrication process for realizing parallel-path FlexConnects is simpler and hence more cost effective. Another advantage of FlexConnects over G-Helix interconnects is their redundant design. Finally, simulations were performed to compare the thermomechanical reliability of single-path FlexConnects (same beam cross-section area as parallel-path FlexConnects) against parallel-path FlexConnects. It was seen that the $N_{50\%}$ life of the single-path FlexConnects was $1/10^{th}$ that of the parallel-path FlexConnects, clearly highlighting the advantage of using multiple electrical paths as part of the compliant interconnect design.

8.2 Contributions

The following contributions have been achieved through this research:

- An innovative parallel-path approach for compliant interconnects to improve electrical performance without compromising on mechanical reliability is developed. The concept is generic in nature and can be adapted to most other compliant interconnect technologies being pursued. The concept could be extended to other mechanical structures in an electronic package which experience displacement controlled loading.

- A fabrication process which facilitates cost-effective, high-yield, and uniform fabrication of free-standing compliant interconnects is developed. A sacrificial layer process with up to two masking steps are utilized as part of the fabrication process.
- A variable compliance approach is developed so that compliant interconnects can meet both electrical and mechanical performance requirements. Such a concept can applied not only to compliant interconnects but also to other first / second level interconnects.
- Critical factors which impact assembly yield of free-standing compliant interconnects are identified and an assembly process recipe for free-standing compliant interconnects is developed with 100% yield on assembly achieved.
- The work augments the limited data available in published research on reliability of compliant interconnects at a fine pitch.
- Using the concepts developed an innovative compliant interconnect called FlexConnects was developed which overcomes the limitations of the current state-of-the-art compliant interconnects. FlexConnects are more cost effective and have improved electrical performance without compromising on the mechanical performance of the interconnects. As the fabrication of FlexConnects is based on lithography and electroplating technologies, it can be integrated into wafer-level fine-pitch batch processing. The fabrication technique developed for FlexConnects allows for a more cost effective implementation of compliant interconnects by utilizing one to two masking steps and corresponding electroplating steps. Other advantages of this technology are: 1) The compliant interconnects will exert minimal force on the die pads, and therefore, will not crack or delaminate the low-K dielectric material on the die 2) The interconnects will not require an underfill to accommodate the CTE mismatch between the die and the organic substrate, and as no underfill is used, the interconnects will be easily reworkable 3) The interconnects can be fabricated at the wafer-level and therefore, can be potentially cost effective Also, as the interconnect

fabrication uses conventional wafer fabrication infrastructure, there are no additional equipment/infrastructure costs 4) As the interconnects are fabricated using lithography and electroplating the interconnect dimensions and shape can be varied across the chip to accommodate the electrical, and mechanical requirements 5) Lead-free solder can be employed for the interconnect assembly to substrates, and therefore, the technology is environmentally friendly.

The concepts developed in this dissertation allow compliant interconnect to address the needs of first level interconnects over the next decade. This would eliminate a bottleneck that threatens to impede the exponential growth in microprocessor performance. Also, the concepts developed are generic in nature and not limited to only compliant interconnects and can be extended to other aspects of electronic packaging for improved electrical performance and/or mechanical reliability.

8.3 Recommendations for Future Work

During the course of this work, other gaps are identified that require investigation or further improvement. Some recommendations for future work are as follows.

- A topological optimization approach can be adopted to develop innovative new designs for compliant interconnect. The current FlexConnect design is based on [Zhu 2003] in which the geometric dimensions of the interconnect are optimized. A topological optimization approach would optimize the shape of the interconnect and could result in alternate interconnect geometries.
- The multiple-path approach can be further investigated to realize compliant interconnect designs which have improved mechanical and electrical performance characteristics In this work, a compliant interconnect design with only two electrical paths is explored. However, more than two paths is possible as shown in Figure 8.1. In employing these multiple electrical paths, the trade-off between manufacturability and number of electrical paths will need to be explored.

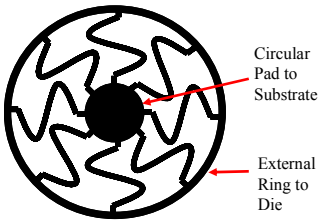


Figure 8.1: Alternate Interpretation of Multiple Electrical Paths

- Experimental characterization of the electrical parasitics of parallel-path FlexConnects over a range of frequencies needs to be performed. The electrical behavior of the compliant interconnect when used in a electronic package needs to be studied through modeling and experiments. The 3D structure of the compliant interconnects adds an additional discontinuity to the signaling path between the die and the substrate. Hence, in addition to reducing the parasitics of the compliant interconnects, the interconnect design may need to be modified to match the silicon and package transmission lines. Detailed modeling of the transition is therefore required.
- Experimental characterization of the electrical and mechanical properties of thin film materials like copper which are employed in the compliant interconnect can be performed.
- A nanoindenter can be used to apply a repetitive displacement on the interconnect in the out-of-plane direction to understand its fatigue behavior. To characterize the fatigue behavior of the interconnect in the in-plane direction a repetitive displacement in the in-plane direction would be needed. To achieve this, the wafer on which the interconnects are fabricated can be rotated by 90°, holding the wafer on its edge. The indenter can then apply a displacement in the up and down direction simulating planar motion.
- A cost analysis of the parallel-path FlexConnect fabrication process should also be performed.

APPENDIX A

FABRICATION PROCESS FOR G-HELIX INTERCONNECTS

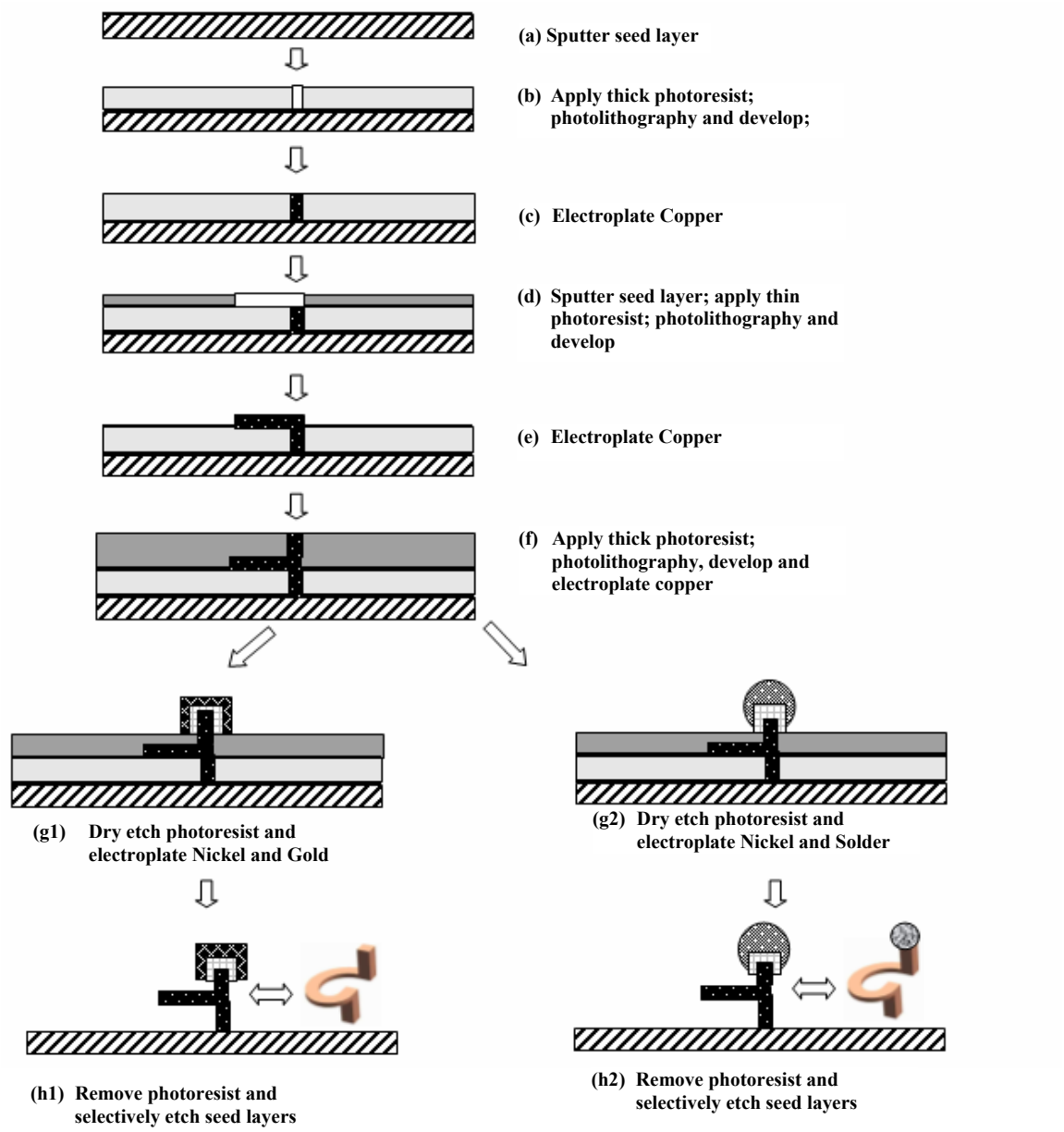


Figure A.1: G-Helix Fabrication Process [Lo and Sitaraman 2004]

APPENDIX B

MATERIAL PROPERTY DATA FOR FEA MODELS

Table B.1: Material Properties for Silicon Die [Hanna et al. 1999]

Material Property	Value
CTE (α)	2.6 ppm/^{o}C
Poisson's Ratio (*v)*	0.25
Young's Modulus (E) at 0°C	120.85 GPa
Young's Modulus (E) at 50°C	114.85 GPa
Young's Modulus (E) at 100°C	109.85 GPa

Table B.2: Material Properties for FR4 Substrate [Hegde 2003]

T, °C	30	95	110	125	150	270
E_x (MPa)	29400	28100	27800	27500	27000	24600
E_z (MPa)	29400	28100	27800	27500	27000	24600
E_y (MPa)	2000	2000	1880	1700	1400	880
ν_{xz}	0.136	0.136	0.136	0.136	0.136	0.136
ν_{xy}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
ν_{yz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
α_x (10^{-6}/°C)	11	11	11	11	11	11
α_z (10^{-6}/°C)	11	11	11	11	11	11
α_y (10^{-6}/°C)	27	30	32	35	40	114

Table B.3: Material Properties for Copper [Iannuzzelli 1991].

Temperature (°C)	E (GPa)	ν	α (10^{-6}/°C)
27	121.0	0.3	17.3

38	119.0	0.3	17.3
93	117.0	0.3	17.3
149	115.0	0.3	17.3
204	112.0	0.3	17.3
260	110.0	0.3	17.3

Table B.4: Stress-Strain Relationship for Copper [Iannuzzelli 1991].

Strain	σ (MPa) At 27°C	σ (MPa) At 260°C
0.001	121	110
0.004	186	179
0.01	217	214
0.02	234	231
0.04	248	245

Table B.5: Constants for Anand Model for 96.5Sn/3.5Ag solder [Wang et al. 2001].

Meaning	Constants for Anand's Model
s_o (MPa)	39.09
Q/R (K)	8900
A $(\sec^{-1})$	2.23×10^4
ξ	6
m	0.182
h_o (MPa)	3321.15
$\hat{s}$ (MPa)	73.81
n	0.018
a	1.82

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